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A MAJOR PERFORMANCE UPGRADE TO THE TRANSVERSE FEEDBACK SYSTEM AT THE ADVANCE PHOTON SOURCE*

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Abstract

With the success and reliability of the transverse feedback system installed at the Advance Photon Source (APS), a major upgrade to expand the system is under way. The existing system is operating at a third of the storage ring bunch capacity, or 432 of the available 1296 bunches. This upgrade will allow the sampling of all 1296 bunches and make corrections for all selected bunches in a single storage ring turn. To facilitate this upgrade a new analog I/O board capable of 352 MHz operation was developed along with a revolution clock cleaning circuit. A 352MHz clock cleaning circuit was also required for the high-speed analog output circuit to maintain data integrity to the receiving DAC unit that is 61m away. This receiving DAC unit will have its transceiver data rate upgraded from 2.3Gbps to about 7Gbps transmitted over a fiber optic link. This paper discusses some of the challenges in reducing the clock jitter from both the system P0 bunch clock and the 352MHz clock along with the necessary FPGA hardware upgrades and algorithm changes, all of which is required for the success of this upgrade.

INTRODUCTION

The Advanced Photon Source (APS) experiences beam instabilities in both the transverse and longitudinal planes. The P0 feedback system, in its initial version, will correct these instabilities in a bunch pattern that has up to 24 bunches. This is accomplished by using a pick-up stripline, drive stripline, four drive amplifiers, a 3-tap comb filter for front-end signal conditioning, and an Altera PCIe Stratix II GX FPGA-based development board coupled with a Coldfire CPU. The Coldfire CPU uses EPICS [1] with RTEMS [2] for all the remote monitoring and control. Figure 1 shows a block diagram of the feedback system. This paper discusses FPGA performance, added features and modifications, as well as the imminent upgrade.

SYSTEM DESCRIPTION

The current system consists of a pick-up stripline, a front-end signal-processing unit, an Altera PCIe Stratix II GX FPGA-based development board, drive amplifiers, and a driver stripline.This system has been described in detail [3]. Figure 1 shows a block diagram of the current system without the remote DAC hardware. At the core of the FPGA processor are the 864 32-tap FIR filters running at 117.3 MHz. The algorithm used for the filter is based on the least square fitting method to determine filter coefficients [4]. The pickup and drive striplines are located in different locations of the storage ring, which is a major issue for the Y-channel since the distance between pickup and drive is seven sectors, or about 188 m, apart. A remote DAC linked to the main transverse feedback system via high-speed fiber optic cable utilizing a real-time data transfer protocol. Figure 2 shows the addition of the transceiver in the main transverse feedback chassis used to connect the remote DAC chassis.

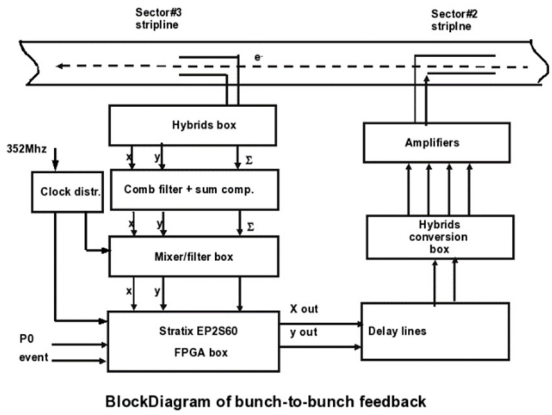

Figure 1: Block diagram of the feedback system.

CURRENT SYSTEM AND LIMITATIONS

The current FPGA system described above has been very successful for the Advanced Photon Source as it has been detailed in a previous paper [5]. This system is limited to 324 or 432 buckets depending on the operating frequency of 88 or 117.3 MHz that's configured for a particular bunch pattern. With the proven success of this system, an opportunity to expand the transverse feedback system to encompass all 1296 buckets has been proposed. This would require the system to operate at the full storage ring frequency of 352 MHz. At 432 buckets, the system is operating at 117.3 MHz, which is near the limitation of the ADC/DAC interface to the FPGA. The current ADC has a maximum sample rate of 125 MHz while the DAC can perform at 150 MHz. The current FPGA (Stratix II GX) is limited to a maximum transceiver rate of 6.376 Gbps of which 2.3 Gbps is needed to transport data to the remote DAC at system clock rate of 117 MHz. To transport data to the remote DAC with a system clock rate at 352 MHz, the transceiver needs to triple its transmission rate from 2.3 Gbps to 7.04 Gbps, which is beyond the Stratix II GX chip's capabilities. The current ADC and DACs are also not sufficient for 352-MHz operation. One solution is to have several ADCs and DACs in parallel to achieve 352-MHz operation. While standard methods can be used to multiplex the ADC front end, it becomes very complicated to mux several DACs to generate a 352-MHz analog control signal. This option also requires more board space,

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a minimum of three ADCs and three DACs, and would require a larger power supply. For the transverse feedback system with two channels, a total of six ADCs and six DACs would be needed. A simpler option is to have a single ADC/DAC pair per channel, which saves on space and power consumption.

One of the biggest hurdles that this upgrade overcame was the jitter in the 352-MHz RF clock and the jitter in the P0 timing trigger. This has not been an issue at the Advanced Photon Source in the past because the existing digitizing systems were running at sub-harmonics of the clock (e.g., 88 MHz, 117.3 MHz, 176 MHz), which precluded the possibility of sampling the full 1296 buckets in the storage ring. This jitter would cause the transverse feedback system to skip to an adjacent bucket with undesirable results. This issue had the potential to put this enhancement on hold.

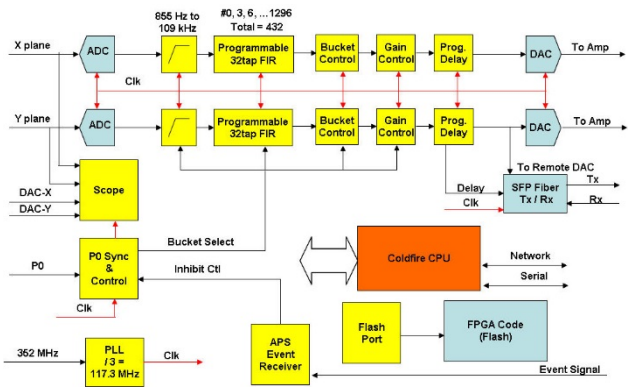

Figure 2: FPGA block diagram of the P0 feedback.

Due to budget constraints, the project upgrade was limited to a similar size Altera development board that was required to have all same ports in order to be a drop-in replacement, but the closest drop-in that Altera provided was a Stratix IV GX Development Kit [6], which has two HSMC and PCIe connectors but no SFP cages. It was necessary to move to the Stratix IV GX chip platform for the higher clock rates needed for this enhancement, and the number of FIR filters tripled as seen in Table 1.

The Stratix II GX could only accept a 500-MHz clock input on an I/O pin and a 500-MHz (max) internal clock speed. Compiling the Stratix II GX for 352-MHz operation failed to meet internal timing specs because there was not enough ceiling between 352 MHz and 500 MHz. With the Stratix IV GX chip, the clock ceiling in the FPGA fabric is high enough to meet the timing requirements of this project. Since the Stratix IV GX did not come with a SFP cage for the optical transmitters, a PCI card was developed with SFP cages that would plug into the Altera development kit's PCIe connector. Testing was performed with this configuration but since the PCIe specification is only good for 5.0 Gbps (Gen2), and this upgrade needed push data at 7.04 Gbps through a card edge connector, concern whether or not the transceiver could be adjusted to go beyond the PCIe specifications. The PCIe to SFP+ adapter board adds about 25 mm to the signal trace but this signal is a point-to-point connection, so signal degradation will be at a minimum. However, this adapter card was tested at the current 2.3-Gbps transfer rate with no data loss. It was questionable whether or not this would work at 7.04 Gbps rate needed at 352MHz operation. Using new SFP+ transceiver capable of 8.5 Gbps will require a performance test with the Finisar transceiver [7] capable of 8.5 Gbps with bi-directional data links to be tested first. A transceiver produced by Avago [8] may also be considered for testing.

Table 1: Possible Bucket Modes

88 MHz	Samples only 324 buckets 1) 324 mode 2) Hybird mode 3) 648 FIR filters needed
117.3 MHz	Samples only 432 buckets 1) 24 singlet mode 2) Hybird mode 3) 864 FIR filters needed
352 MHz	Samples only 1296 buckets 1) Any bucket configuration 2) 2392 FIR filters needed

These limitations mentioned above in the current transverse feedback system using the Altera Stratix II GX PCIe development kit prompted the need to upgrade the system. This kit only has two HSMC (High Speed Mezzanine Card) ports, one that is populated with a Coldfire CPU daughter board and the other with a two-channel ADC/DAC board. The problem with the Altera development boards is that they only have two HSMC connectors, which limit your options. The need for a 14-bit 400MSPS ADC and DAC chip to run at the 352 MHz is required. These chips use differential LVDS for the data and clock pins so there was a limitation of only one ADC and one DAC on one HSMC connector.

HARDWARE UPGRADES

With the Altera development boards, it was only possible to use the HSMC Data Conversion Board, which is a single HSMC board that has two ADCs (125MHz) and two DACs (150MHz) because they were single ended lines. The single ended lines allowed up to four chips with a 14-bit buses to connect to the HSMC connector. But the speeds required for operations at 352MHz requires differential data lines, or LVDS signals, limiting the HSMC connector to only one ADC and one DAC. It was obvious that two HSMC boards was necessary to maintain a two-channel system with two ADCs and two DACs for 400MSPS operations. Discovered an alternative main board that had more than two HSMC connectors and it was the Terasic TR4 FPGA Development Kit [9], which also has a Stratix IV GX chip

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installed on it. This board has six HSMC connectors, which provided the flexibility of installing two 400MSPS Data Conversion boards. The remaining four connectors configured for a Coldfire CPU board, a Transceiver to SMA board, an eight cage SFP board and then an Event Receiver interface board.

The 400MSPS boards were specially designed for this project and the engineering was done buy System Level Solutions, Inc (SLS). Four main components that is install on this board are, ADC (ADS5474A), DAC (DAC5675A) and two Clock Jitter Cleaner (SI5317A) chips. The clock jitter cleaners also provide a nice means to adjust the clock phase to fine-tune the ADC or the DAC to the FPGA fabric.

The existing data conversion board (DCB) [10] has a HSMC connector that connects to the main Altera development board. This DCB has two ADC channels and two DAC channels. The maximum sample rate for the ADC is 125 MHz at 12bits and the DAC maximum sample rate is 150 MHz at 14 bits. For this upgrade this system needs to operate at 352 MHz, which these devices will not be able to accommodate.

The APS tried to design a 352MHz DCB with two ADCs and two DACs on a single HSMC board but could not meet the timing constraints in the Altera Startix IV development board. Due to the limited pins on the HSMC connector and since the data lines were LVDS based, the HSMC could only support one ADC and one DAC. An attempt to use Double Data Rate (DDR) to combine two ADCs on the same set of LVDS lines proved to be difficult in passing the timing constraints on the Stratix IV. Apparently, the design was pushing the timing limits with the needed 704MHz clock need for the DDR to separate the two ADCs. Once that was done each ADC's data was in DDR format so this had to be un-packed also. This was not an issue with the DAC chip since the DAC had two channels and the data was in DDR format. This design was running out of board space and becoming very complicated in the board layout. It became apparent that another design solution for a 352MHz DCB was in order.

The first issue was the main Altera Stratix IV development board only having two HSMC connectors. If this board had three then the logic and the complexity of the design could be reduced to a single ADC and a single DAC on one HSMC board. As mentioned above, search discovered the Terasic TR4 board with a Stratix IV chip with six HSMC connectors. The TR4 has much to offer but it does not have any Small Form-Factor Pluggable (SFP) cages for fiber optic transmitters/receivers needed for this project. Terasic does offer a HSMC board (SFP HSMC) [11] that has eight SFPs, four being LVDS base while the other four are transceiver based. The TR4 is limited on SMA clock inputs and this project needs an extra differential clock input. Terasic offers a simple HSMC board called the HSMC-XTS [12], which has several transceiver circuits connected to a pair of SMA connectors. This board has provision for SMA clock input and SMA clock output were this upgrade will be using the clock input for this project. This system will continue to use the Coldfire CPU platform, which the APS has HSMC adapter already designed. A new Event Receiver interface board was design to implement a Taxi chip decoder verses using firmware to separate the clock and data signals. This was necessary due to the Stratix IV GX dropping bits that was not an issue with the Stratix II GX chip.

A major design consideration in developing the new DCB is how to deal with an ADC`s high sensitivity to jitter from the sampling clock when digitizing analog signals at high sampling rates. Long-term testing of the LLRF clock signals at APS have shown that the existing clock contains a number of spurs in the -75 to -95 dbm range and a prominent spur at 1 MHz, which appears to be a product of the 10-MHz reference synthesizer. For the vast majority of operations within APS, the LLRF clock is sufficiently clean, but for direct sampling at 352 MHz, the existing clock must be cleaned further. The new DCB will provide one 14-bit 400 MSPS Analog Devices ADCs and one 14-bit 400 MSPS DAC, thus providing an independent ADC and DAC signal channel. In order to maintain the ~12-bit ENOB of the ADC at 352 MSPS, the LLRF sample clock must have the lowest jitter possible. To that end, a high-speed RF comparator connected to a jitter cleaner board (SI5317-EVB) which provides clock distribution for the main FPGA clock input and another output to connect to the transceiver clock input. The jitter cleaner chip provides two independent LVDS outputs at frequencies up to 352 MHz. In addition to this jitter cleaner circuit each 400MSPS DCB has two Si5317, one for the ADC and the other for the DAC with each output capable of incrementing and decrementing its phase offset from the input reference clock in 180-ps steps.

SOFTWARE IMPROVEMENTS

To facilitate system diagnostics and tuning we also added some EPICS process variables for both ADC inputs and DAC outputs in addition to some firmware features.

For each sample, we define a 3-bit control pattern as shown in Table 2. These control functions are programmable for purposes such as timing alignment, AC coupling effect compensation of DAC output, and bandwidth matching of the amplifiers. Option 000 or 111 will set the DAC output to zero volts. Option 001 simply passes the data though to the DAC, while option 010 negates the data before going to the DAC. Options 011 and 100 are separate registers holding some preprogrammed value. Option 101 toggles data from the previous bucket for the current bucket, and option 110 stretches the data from the previous bucket into the current bucket. These last four options ignore the processed data from the FIR filters.

Developed high-level software to facilitate machine studies, e.g., a graphic interface for loading and saving DAC output control patterns; generating FIR filter from lattice files; and saving, reviewing and loading FIR filters. This software is based on the Tcl/Tk interpreter using the SDDS Toolkit.

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Table 2: DAC Output Control Bit Patterns

000	Zero volts out
001	Normal processed data
010	Negate processed data
011	Programmable negative output value
100	Programmable positive output value
101	Toggle (negate) data output
110	Stretch (repeat) data output
111	Zero volts out

FUTURE PLANS

The previous configuration at 117.3MHz could only correct 432 bucket due to being only a third of the storage ring frequency of 352MHz. At the frequency of 117.3MHz the fiber link only had to operate 2.3Gbps using basic 8b/10b protocol. The transmitter transceiver operated with 16-bit data bus at 117.3MHz while the receiver transceiver was configured to output an 8-bit data word running at 234.6MHz. This improved the reliability of the data transmission that the receiver would not have to deal with byte swapping. However, at the time of this writing a new configuration is be developed to accommodate data at 352MHz. In this configuration, the data bus to and from the transceivers will both be 32-bits wide. An alignment algorithm on the receiver circuit needs send data to the DAC that will not interfere with the beam, which might bump a bunch out of orbit.

Due to the added complexity of the remote slave DAC an EPICS IOC will be installed in the slave unit to monitor the fiber link and perform any realignment if necessary.

This upgraded system is scheduled to be installed January 2018, which at that time a system performance test will be perform to verify normal operations.

CONCLUSION

The P0 feedback system has proven to be very flexible in that it was easy to adapt when the need arose, e.g., increasing the number of buckets and adding a remote DAC function. However, the pervious configuration could not accommodate for all 1296 buckets limiting what bunch pattern could be used. The preliminary test data have shown some promise that this system can stabilize 1296 bunches in both the horizontal and vertical planes at the APS and possibly function as a bunch cleaner.

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