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uSOP: AN EMBEDDED LINUX BOARD FOR THE BELLE2 DETECTOR CONTROLS

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Abstract

Control systems for scientific instruments and experiments would benefit from hardware and software platforms that provide flexible resources to fulfill various installation requirements. uSOP is a Single Board Computer based on ARM processor and Linux operating system that makes it possible to develop and deploy easily various control system frameworks (EPICS, Tango) supporting a variety of different buses (I2C, SPI, UART, JTAG), ADC, General Purpose and specialized digital IO. In this work, we describe features and architecture of uSOP board and its deployment as a monitoring system for the Belle2 experiment, presently under construction at the KEK Laboratory (Tsukuba, Japan).

INTRODUCTION

In the last few years companies and no-profit organizations, exploiting availability of powerful microprocessors at low price, have developed various Single-Board Computers (SBCs) to fullfill different users requirements. Projects like Raspberry Pi [1], BeagleBone Black [2], are only some examples of this trend. Main advantages of SBCs usage are low price, good performance, compactness and widespread operating systems (e.g. Linux).

Despite such advantages a common SBC is not suitable "as is" for a custom task. In industrial or scientific fields there are standards or form factor to be compliant with, electronic interfaces or custom busses to adopt, and integration of an off-the-shelf SBCs is not so easy.

The availability of electronic schematics and PCBs with Open-source Hardware license for various SBCs overcome these integration problems making feasible the implementation of a custom SBC composed by a central core inherited from off-the-shelf SBC (microprocessor, static RAM, flash memory) and various peripherals required to integrate a new architecture into a specific environment. With this approach the custom SBC user will keep exploiting all supported tools and software provided by SBC community: a very powerful help in satisfying all constraints enforced by his scientific or industrial environment.

THE USOP BOARD

The uSOP board (Fig. 1) is derived from BeagleBone Black Open-source Hardware project. It has been designed as expandable platform to run applications in controls and monitoring of sensors, detectors and other complex scientific research equipment.

Physical Layout

The board has an Eurocard 3U form factor and it is possible to use it in stand-alone mode or as a plug-in unit inside an Eurocard crate. It is powered by an external regulated supply at 5V with a typical power consumption of less than 3W.

The on-board power distribution has been segmented to provide a clean supply for acquisition peripherals. The noisy digital domains are powered with high-efficiency Point-Of-Load switching regulators while linear regulators supply the more demanding, high-speed I/Os like USB and Ethernet. Thermal shutdown, over-current and short-circuit protection are guaranteed by design for safe operation in hostile and limited access environments [3].

Hardware Features

The processor of uSOP board is the Texas Instrument Sitara AM335x (Cortex-A8 SoC) which runs up to 1 GHz clock rate. It provides a large set of serial busses: I2C, SPI, CAN, USB and it is also equipped with Ethernet ports, mass storage interface and 12-bit ADC. Two coprocessors (Programmable Real Time Units – PRU) are also available.

In the present version, uSOP has 512 Mbyte RAM and 4 Gbyte of mass storage by on-board eMMC. Dual instances of SPI, I2C and UART are available and all of them are galvanically isolated with separate supplies (5V, 12V) in order to power remote sensors and acquisition boards with ADCs, DACs and other peripherals. JTAG protocol is also available by software using a set of galvanically isolated GPIO pins. Two 8-bit expansion connectors allow usage of additional GPIO pins for custom protocols implementation and four buffered 12-bit ADC are available to the user.

uSOP board has been designed to run in harsh and unattended environments and the most critical system operations can be performed remotely by a dedicated out

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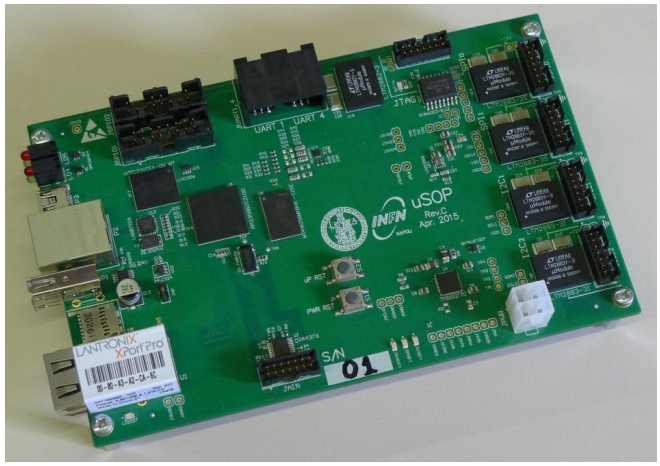

Figure 1: The uSOP board.

of band LAN connection that operates independently from the main processor. This is done by a compact self-contained networking module [4]. It provides in the package of an Ethernet socket a server running uCLinux with a minimal footprint of RAM and Flash. An I2C software controller drives an external IO expander which allows the user to reset and power cycle the uSOP board, and modify the boot sequence of the processor as well. Through the UART, it is also possible to redirect the uSOP console on the LAN.

OPERATING SYSTEM

Boot Features

User can choose either first stage and second stage boot media. uSOP uses U-Boot [5] as Linux bootloader and, as far as a first stage boot is concerned, it can be loaded from eMMC, micro-SD, UART (via XModem/YModem protocol) or Ethernet (DHCP + TFTP). The second stage boot is performed by U-Boot that can fetch Linux kernel image from eMMC, micro-SD or Ethernet (TFTP).

Selection of first stage boot media can be done by the network with the Lantronix XPort management module that offers a command line or EPICS IOC to accomplish this task. Second stage boot selection can be performed by U-Boot command line console available remotely through the network management module.

Linux Distribution

Linux Debian has been selected as preferred distribution for uSOP board. Sitara AM335x processor is supported by BeagleBoard.org Foundation that provides open-source Linux kernel drivers and patches. Using an image-builder scripts set it is possible to generate (on a separate PC) a root filesystem (rootfs) image based on last ARM Linux kernel with a selection of packages ports. The rootfs image is suitable for eMMC/micro-SD installation or network booting.

The hardware features and resources of the uSOP board make it possible to use language compilers and interpreters directly on-board without need of cross-compilation on a separate PC. Thanks to Linux Debian, uSOP users experiences a “fully fledged” Linux system with a huge selection of packages and libraries already available in binary format by official network repositories without need to search, compile and install each software dependencies.

EPICS Framework

Last EPICS base (R3.15.5) is selected for uSOP and, also in this case, EPICS IOC development can be done directly on board using C/C++ on-board compiler and related utilities.

During last development activities uSOP board runs EPICS IOC written in Python using PCASpy [6] and it is used in other environments with StreamDevice [7] components. Some successfully tests have also been done with compilation, installation and usage of EPICS V4.

THE BELLE2 EXPERIMENT

The BelleII detector [8] is currently under construction at the SuperKEKB electron-positron collider at the KEK Laboratory (Tsukuba, Japan). As a major upgrade of the forerunner Belle experiment at the KEKB collider, the BelleII detector has been improved to make measurements of CP-violating asymmetries in rare B meson decays, to achieve precision determination of CKM parameters, and to perform sensitive searches for lepton flavour violation and lepton number violation in rare and forbidden B and D decays.

The BelleII Electromagnetic Calorimeter (ECL) is divided in a barrel and two anular endcap regions, named forward and backward following the asymmetric design of the low-energy (positron, 4 GeV) and high-energy (electron, 7 GeV) collider rings. CsI(Tl) was chosen as the scintillation crystal material in all regions, due to its high light output at an affordable cost. Light yield does change with temperature [9] and crystals are strongly hygroscopic and they can be severely damaged by humidity [10]. Forward and backward endcaps are made

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of 2112 CsI(Tl) crystals, arranged in 16+16 sectors. Each sector is equipped with three thermistors and an active humidity probe for a total of 128 analog channels.

USOP DEPLOYMENT IN BELLE2 EXPERIMENT

Hardware Layout

Temperature and relative humidity in the two BelleII ECL endcaps are monitored by a uSOP-based network [11]. Each endcap is read out by four uSOP boards placed in a 19-inches 6U crate (Fig. 2). Each uSOP unit is hosted in a 6U carrier box with ADC unit for readout of thermistors and humidity probe readout. The 6U crate is equipped with a power backplane and redundant power supplies in order to provide regulated 5V to each uSOP board.

Figure 2: uSOP crate for BelleII monitoring system.

ADC Main Features

For temperature and humidity readout the Linear LTC2983 [12] 24-bit, ΔΣ ADC has been selected. It can measure temperature using the most common sensors (thermocouples, RTDs, thermistors, and diodes) and it includes all necessary active circuitry, switches, including processing hardware to perform measurement algorithms, and mathematical conversions to determine the temperature for each sensor type.

LTC2983 also provides 10 differential or 20 single ended buffered inputs with SPI interface for configuration and readout and it is fully compliant to slow control and monitoring requirements in terms of speed and precision.

Software Deployment

A specialized EPICS IOC has been developed to interface uSOP with LTC2983 ADC through SPI bus. Each temperature and humidity value is published on BelleII EPICS network and stored in an EPICS Archiver.

Data Visualization

Control System Studio (CSS) [13] is the visualization tool selected by BelleII. ECL temperature and humidity values are monitored with various control panels.

Different levels of detail are provided to user by means of multiple views of the collected data. In “bird's eye” view (Fig. 3) a single snapshot of last collected data is displayed and each sector of a selected endcap (forward or backward) is labeled with temperature and humidity metrics. Another view is available to live monitor a single ECL sector over time in order to highlight critical trends. The interface with historical data, stored in EPICS Archiver database, is provided by CSS Data Browser that makes possible data inspection over an arbitrary time period (Fig. 4).

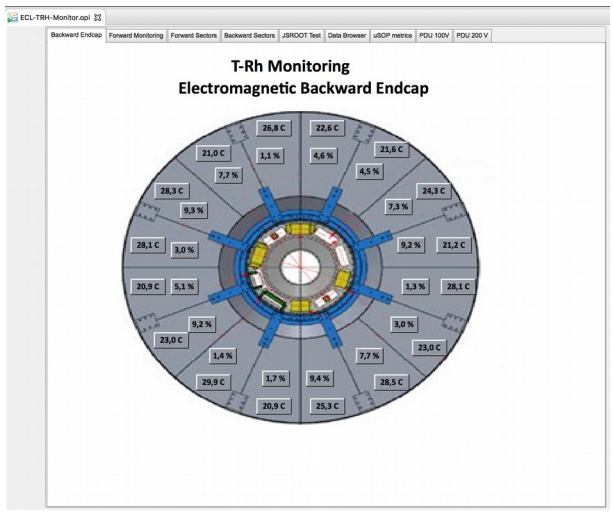

Figure 3: “Bird's eye” view for a selected endcap.

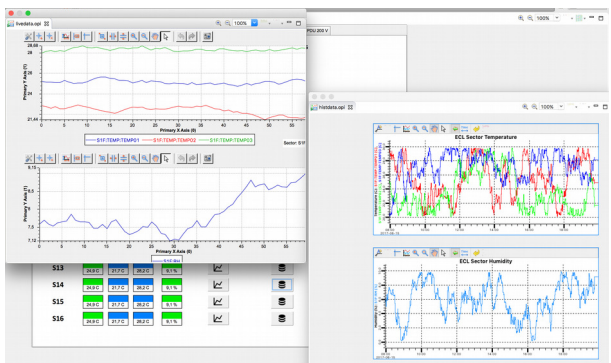

Figure 4: Live monitor and historical data plot of selected ECL sector.

CONCLUSIONS

uSOP board is a Linux SBC with hardware and software features specifically designed for scientific and industrial environments. The adoption of a fully fledged Linux distribution plays a key role in fast development of software solutions, breaking down the learning curve of a typical custom Linux distribution. At KEK laboratory, uSOP has been deployed in the monitoring of environmental parameters (T, Rh) for the endcap regions of the ECL and it has showed its reliability and robustness

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running for more than one year in unattended and continuous uptime.

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