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DEVELOPMENT OF A NEW DATA ACQUISITION SYSTEM FOR A PHOTON COUNTING DETECTOR PROTOTYPE AT SOLEIL SYNCHROTRON

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Abstract

Time-resolved pump-probe experiments at SOLEIL Synchrotron (France) have motivated the development of a new and fast photon counting camera prototype. The core of the camera is a hybrid pixel detector, based on the UFXC32k readout chips bump-bonded to a silicon sensor. This detector exhibits promising performances with very fast readout time, high dynamic range, extended count rate linearity and optimized X-ray detection in the energy range 5-15 keV. In close collaboration with CRISTAL beamline, SOLEIL's Detector, Electronics and Software Groups carried out a common R&D project to design and realize a 2-chips camera prototype with a high-speed data acquisition system. The system has been fully integrated into Tango and Lima data acquisition framework used at SOLEIL. The development and first experimental results will be presented in this paper.

CONTEXT

The goal of the project was to develop a complete acquisition system for a detector prototype based on the UFXC32k readout chip [1]. It consisted of design and realization of the specific electronics hardware, firmware and software that allows performing pump-probe experiments at SOLEIL as depicted in Figure 1 and described in [2].

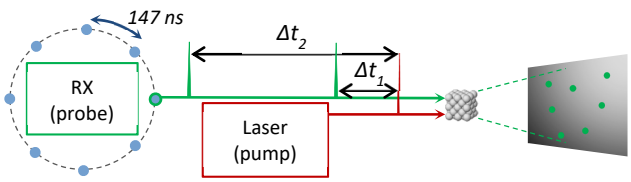

Figure 1: Pump and probe-probe experiment.

The principle of the experiment consists of having laser pulses, at half the frequency of X-ray pulses, to excite a sample (Pump). X-ray pulses, coming from synchrotron bunch, lighting the sample (Probe). Some preliminary results are given in last section, after description of the detector architecture with main focus on the data acquisition system.

HARDWARE DESIGN

In order to optimize development time of the detector acquisition system, several elements of hardware and open firmware/software framework from the PandABox [3,4,5] platform were chosen, reused and adapted for this project.

We have developed hardware architecture in a compact format for the need of the 2chips detector prototype.

The 3 stages electronics, in Fig. 2, consist of:

- The DETECTOR prototype to host the 2-chips hybrid pixel module.
- The DAQ (Data AcQuisition) Box as readout electronics, designed to be a compact hardware variation of PandABox.
- A server to accommodate the slow control and the storage of the fast throughputs of experimental data.

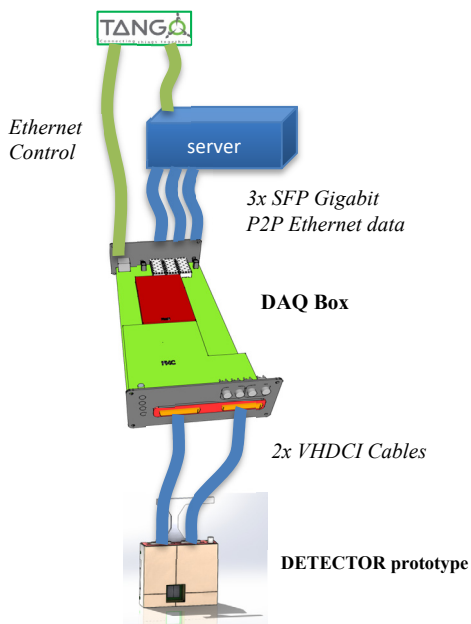

Figure 2: Hardware architecture.

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DETECTOR Prototype

The detector prototype has been developed to host two UFXC32k chips with characteristics shown in Table 1 and covered in details in publications [1,6]. The Detector electronic board was designed to host the detector sensor and interface with the DAQ readout system.

Table 1: Characteristics of the 2-Chip Detector

Pixel size	75 × 75 µm
Number of pixels	256 × 257 pixels (including one column of virtual pixels)
Active detection surface	2× 2 cm²
Inter chip gap	75 µm covered by larger sensor pixels (75 × 112.5 µm²)
In-pixel corrections	Offset (7 bit) and gain (4 bits)
Number of discriminators/pixel	2 thresholds (low, high)
Number of counter/pixels	2 of 14 bits
Camera framerate	20 kfps in 2-bit readout mode

Two high-speed VHDCI (Very-high-Density Cable Interconnect) cables are used to connect the Detector board to the DAQ Box readout electronics.

On the Detector board, special care has been taken in the design for relative electrical delay between LVDS lines from the VHDCI connector to the wire bonded UFXC32k chips (see Fig. 3).

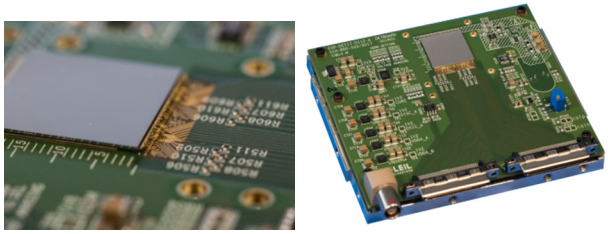

Figure 3: UFXC32k chips integrated on DET board.

The Detector board, powered by an external 5V DC power supply, also manages sensor polarisation (High Voltage up to 150 V) and all the necessary low voltage power supply to the UFXC32k chips for a total power consumption of less than 8 W during the acquisitions.

Voltage and temperature monitoring were added through I2C interfaces toward the DAQ Box.

Compact and light mechanical structure has been designed, as depicted in Figure 4, to ease the installation on the beamlines in embedding the whole system in the experimental environment.

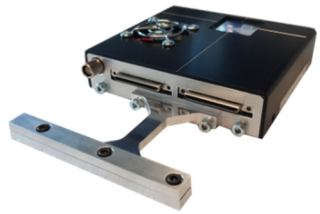

Figure 4: Detector integrated in its mechanic.

The Detector Prototype dimension is 10.5 × 11.5 × 2.5 cm3 with a total weight of less than 500 g.

DAQ Box

The DAQ Box (Data AcQuisition Box) main purpose is to control the UFXC32k chips and readout the image data to the storage server through 3 SFP ports. Moreover this box manages the synchronization with external system such as laser signal for the pump-probe experiment. This box is interfaced with TANGO clients via TCP Ethernet communication.

The electronic DAQ board (see Figure 5) hosting Avnet PicoZed Z7030 module based on a powerful Xilinx Zynq 7030 SoC (System on Chip), is a compact version of the PandABox electronic [4]. It is developed with FMC interface that provides flexibility for different FMC board applications.

Figure 5: Picture of the DAQ board.

To interface the DAQ board with the Detector board, a double width FMC card with a single LPC connector Board has been developed for this specific application.

The DAQ Box mechanicals design (see Figure 6) was designed to ease installation on beamline diffractometer with a size of 17 × 31 × 9 cm3 and a total weight of around 1 kg.

Figure 6: DAQ Box mechanic.

Server

The server used for the first tests of the detector prototype was chosen from standards used at SOLEIL with at least four Ethernet connexions, one for the control network and three for point to point connexions to the DAQ Box. At least 24 GByte of RAM is required to store the incoming data. Future improvements of this system are foreseen.

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FIRMWARE/SOFTWARE DESIGN

PandABlocks open framework [3] and Tango software development for PandABox at SOLEIL were reused to integrate the detector into SOLEIL control system. In addition, a new data streaming mechanism through 3 SFP ports has been developed in the DAQ Box firmware for this project.

The detector settings and the control of the acquisition are controlled by the Tango software over the TCP Ethernet network.

The detector settings consist of global configuration (e.g. discriminators thresholds and settings of the various UFXC ADCs) and pixel configuration (e.g, pixel gain, offset, etc.) .

The control of acquisition is currently implemented with operating modes shown in Table 2.

Table 2: Detector Modes

Software	n images with 2 counters 14 bit + 14 bit
external trigger	n triggered images with 2 counters 14bit+14bit
Pump&Probe	n modulo 2 of triggered pumped&probe images 2 counters 2 bit + 2 bit

The data streaming from the detector to the server storage system was implemented using UDP/IP protocol with point to point Ethernet links over the 3 SFP ports of the DAQ Box to minimize network congestions.

FIRMWARE

The PandABlocks open framework, includes the building scripts and the source code that are required to build the Linux OS for the Zynq ARM core and the embedded TCP server to communicate with the FPGA logic blocks.

As shown in Figure 7, the main development based on this framework was creating specific FMC and SFP FPGA blocks for the detector project.

In the FMC block, a 200 MHz clock domain has been used to comply with the image readout frame rate and not to overcome the FPGA limitations.

The FMC block contains drivers for the signals sequence generation to control the detector with respect to its specific serial communication protocol. This block also retrieves the detector data chunks, build data packets and to dispatch them, in a round robin manner, to three FIFOs. Each detector data packet contains of 1024 Bytes of actual data, chip ID, counter ID, packet number and image number. Dual clock port FIFO has been used to act as buffer and permits the clock domain crossing to the 125 MHz system clock.

The TTL block with TTL inputs are used for the synchronisation of the detector counter collection (start of exposure time) for “external trigger” and “Pump&Probe” modes (shown in Table 1).

The SFP block has been developed upon an OpenCores UDP IP Stack [7] including 3 SFP UDP modules, each sending Gigabit Ethernet UDP/IP frames with data from its dedicated FIFO. Each UDP frame respects a customised format including the frame data identifications information and the associated detector pixel data as described in Table 3.

Table 3: UFXC UDP Frame Data Description

Field	Frame data 1030 Bytes	Values Description
Header	Image count 2 Bytes	The number of the image sent
	Acquisition mode 1 Byte	Acquisition mode used
	Counter H/L 1 Byte	0x00 : counter LOW 0x01 : counter HIGH
	Chip id 1 Byte	0x1A: chip 1 0x2B: chip 2
	udp frame count 1 Byte	Frame number of a given image number
Data	Data 1024 Bytes	Pixel data

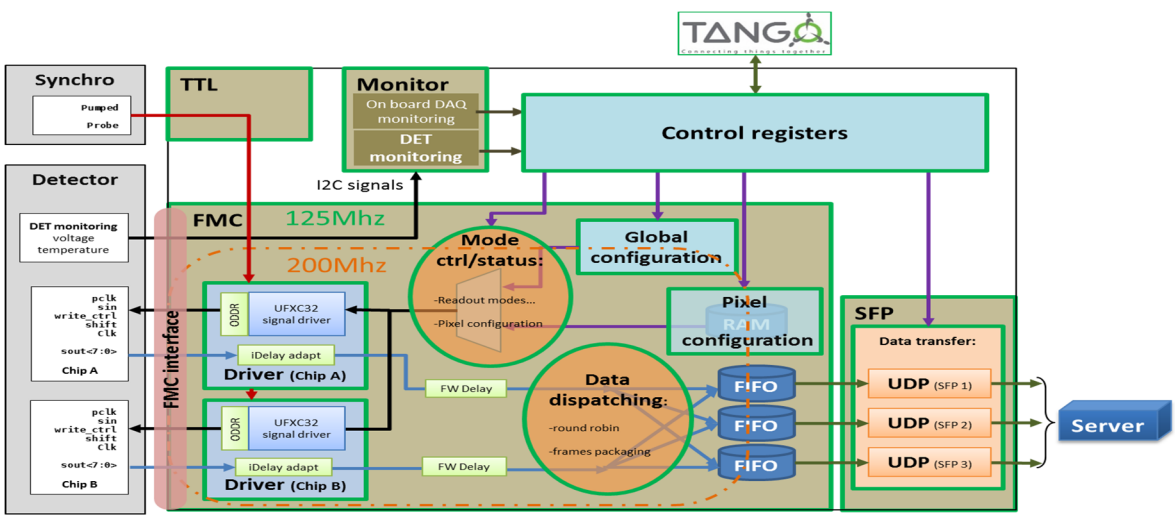

Figure 7: DAQ firmware architecture.

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SOFTWARE

The purpose of the UFXC library is to interface high level clients and the DAQ Box with ASCII communication protocol over TCP Ethernet network. It provides 3 main functions:

DAQ connection & detector monitoring (e.g. open/close connection, set detector global configuration, read DAQ temperatures & voltages); it also includes basic functions to read or write the FPGA registers (simple registers or tables);

Acquisition management (e.g. set acquisition mode, low/high threshold, start/stop acquisition);

Data reading (e.g. set DAQ Box SFPs configuration, image reconstruction).

Figure 8 shows the 3 main functional blocks of the UFXC libraries and their dependencies:

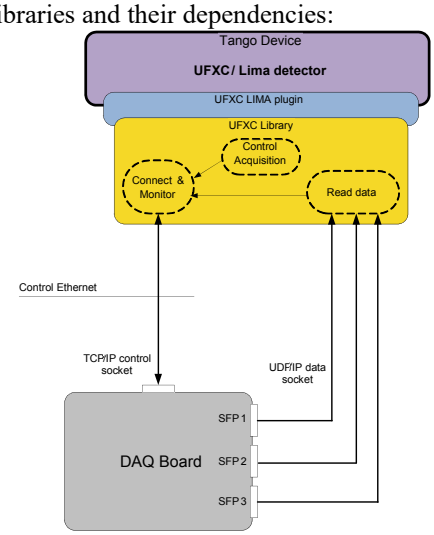

Figure 8: UFXC Libraries Structure.

The development resulted in the standard Tango/Lima [8] interfaces is depicted in Figure 9.

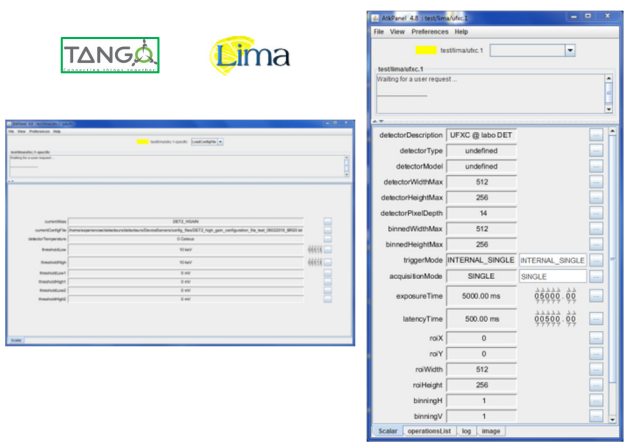

Figure 9: Tango/Lima Graphical User Interfaces.

TESTS AND EXPERIMENTS

Validation Tests

In the development of the complete system, various tests have been conducted such as:

- Electrical test of the various produced boards.
- Firmware individual tests:
  - Tests of emulating detector data with FMC loopback card and analysing transmitted UDP data with python scripts;
  - Tests of detector signal sequence (comparison with NI PXI system);
  - Tests of the communication interface to the detector by writing and reading user defined pixel configurations (e.g. geometrical gradients or random values).
- Software/Firmware integration tests.
- Tests with in Lab with X-ray sources.

All these tests allowed to detect and to fix foreseeable bugs occurring during the development process.

CRISTAL Beamline Experiment

In February 2019, the first test of the detector with the complete acquisition chain has been conducted on the CRISTAL beamline at SOLEIL.

Figure 10 illustrates the electronics installation on the diffractometer. A reference experiment was performed with acquisition of diffraction rings from a PTFE sample. This sample was already studied with other X-ray hybrid pixel detectors (such as XPAD [9]).

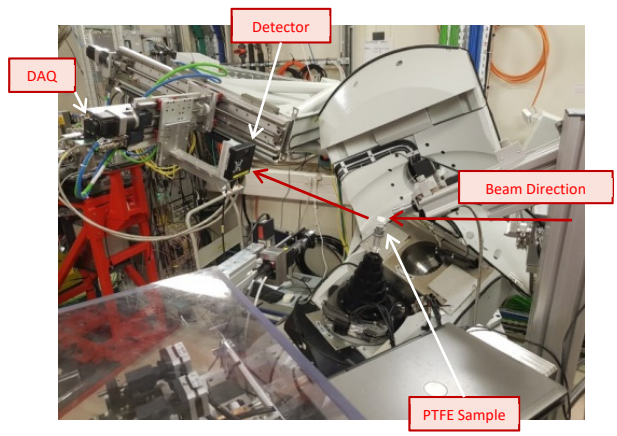

Figure 10: Experimental setup on the CRISTAL beamline.

The images acquired during the tests, as shown on Figure 11, contains: on top, the two counters images of a flat field exposure, used to locate bad pixels and to uniformed the detector pixels response. This enters in the constitution of the detector pixel calibration file (pixel gain, offset …).

The bottom half of Figure 11 depicts the PTFE diffraction rings.

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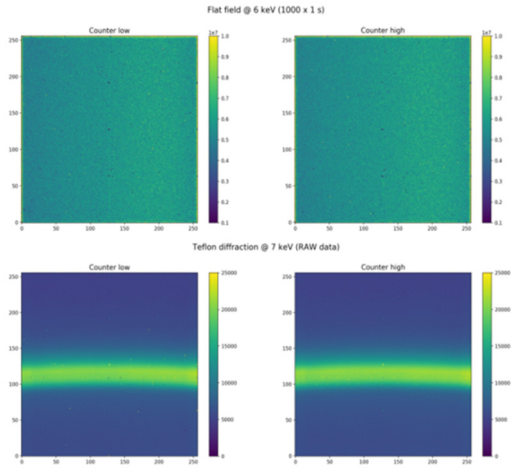

Figure 11: Images of Flat field (top) and PTFE diffraction rings (bottom).

The first results obtained on the beamline featured promising results for the coming pump-probe experiments [10].

CONCLUSION AND PERSPECTIVES

The 2 modules detector prototype with all hardware components has been designed, realized and tested, as well as firmware and control software developments. The full acquisition system has been validated on the CRISTAL beamline [11] at SOLEIL.

Other beamlines at SOLEIL have shown their interests in the UFXC32k detector: ODE beamline has leaded to the development of a new detector prototype with different modules geometry of 1× 4 cm².

Variant of data acquisition modes have been required by the scientists and will be implemented in firmware and software, such as 28 bit per pixel acquisition mode. This mode is to extend exposure time at high beam fluxes without saturating pixel counter dynamics.

This present development is part of a longer term detector program at SOLEIL. Next step consists to develop an 8 modules demonstrator based on the same ASIC.

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