

EVOLUTION BASED ON MICROTCA AND MRF TIMING SYSTEM

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Abstract

For many years our Institute CEA Irfu has had a sound experience in VME and EPICS. For the accelerator projects Spiral2 at Ganil in Normandy (France) and IFMIF/LIPAc at JAEA/Rokkasho (Japan) the EPICS control systems were based on VME. For 5 years our Institute has been involved in several in-kind collaboration contracts with ESS. For the first contracts (ESS test stands, Source and LEPT controls) ESS recommended we use VME based solutions on IOxOS boards. Our close collaboration with ESS, their support and the requirements for new projects have led us to develop a standardized hardware and software platform called Irfu EPICS Environment based on microTCA.4 and MRF timing system. This paper describes the advantages of the combination of these recent technologies and the local control system architectures in progress for the SARAF project.

INTRODUCTION

The CEA Irfu Institute started to use VME in 1983 to upgrade the command control of the Linear Accelerator of Saclay, called ALS, located at Orme des Merisiers very close to Saclay. The associated VME real time system was Versados then VxWorks from 1989. VxWorks was chosen for the accelerator prototype MACSE based on superconductive cavities. In 1993 we came into the EPICS community with the platform VME/VxWorks that we used for different projects and collaborations. For instance, we used this EPICS solution for the collaboration with the Tesla Test Facility at DESY (Germany), for Spiral2 [1] at Caen in Normandy (France) and for the IFMIF LIPAc project at Rokkasho (Japan).

The migration to MTCA.4 was decided in summer 2018. This paper presents the context and the design for this MTCA.4 platform and the application in the SARAF project introduced in [2, 3, 4].

CONTEXT

We started a collaboration with ESS (European Spallation Source) in 2014 essentially based on VME/Linux, IOxOS boards and Siemens 1500 PLC solutions. We were in charge of the control system of the ESS source and LEPT at Catania (Sicily, Italy) and several RF test stands for ESS [5]. The IOxOS Company had already started its migration to MTCA.4 and their acquisition boards presented a definite advantage.

The FPGA Mezzanine Card (FMC) acquisition boards permitted us to upgrade to MTCA.4 by saving the FMC and the cabling.

We noticed that our usual VME companies neglected the VME support. We also felt that IOxOS was becoming more involved in its new orientations, MTCA.4, than in VME. This situation was new.

ESS decided to migrate to MTCA.4 very early on [6]. We could observe their progress on MTCA.4 with the IOxOS boards and the advantages of using both MTCA.4 and the MRF timing system. ESS ICS encouraged us to do such a migration. Our partner SNRC accepted CEA's recommendation to migrate to MTCA.4 for the SARAF control system. Therefore, all together we decided this migration in summer 2018. The CEA team updated and standardized the IRFU EPICS Environment [7] with MTCA.4 solutions based on IOxOS, MRF boards and ESS ICS EPICS drivers to start. See Figure 1. Now, we are beginning to use our own IOxOS EPICS drivers for more flexibility.

MTCA.4 PLATFORM

Generalities

MTCA is an electronic framework for analogue and digital signal processing. MTCA.4 was released as an official standard by the PCI Industrial Manufacturers Group (PICMG) in 2011 and is strongly supported by the xTCA physics groups and electronics manufacturers.

Advantages regarding VME are a larger bandwidth, additional timing and trigger signals in the backplane, introduction of Rear Transition Modules (RTM) allowing to connect cables from the rear and to swap IO and processing boards without the need to remove the rear cables. The RTM can provide low and high speed analogue signals, digital signals, clock signals and management signals.

Crates

We plan to standardize 2 MTCA.4 crate types with several boards. Our first choice is the crate NATIVE-R2, a very compact one.

MCH and CPU boards

The NAT-MCH-PHYS80 offers an 80-port PCIe Gen3 switch and can be combined with the Rear Transition Module with quad-core Intel® Xeon® E3 CPU NAT-MCH-RTM-COMex-E3. Currently, the new PCIe hub module turns the NAT-MCH-PHYS80 into a powerful single-slot solution for management and switching that is available for MTCA.4.

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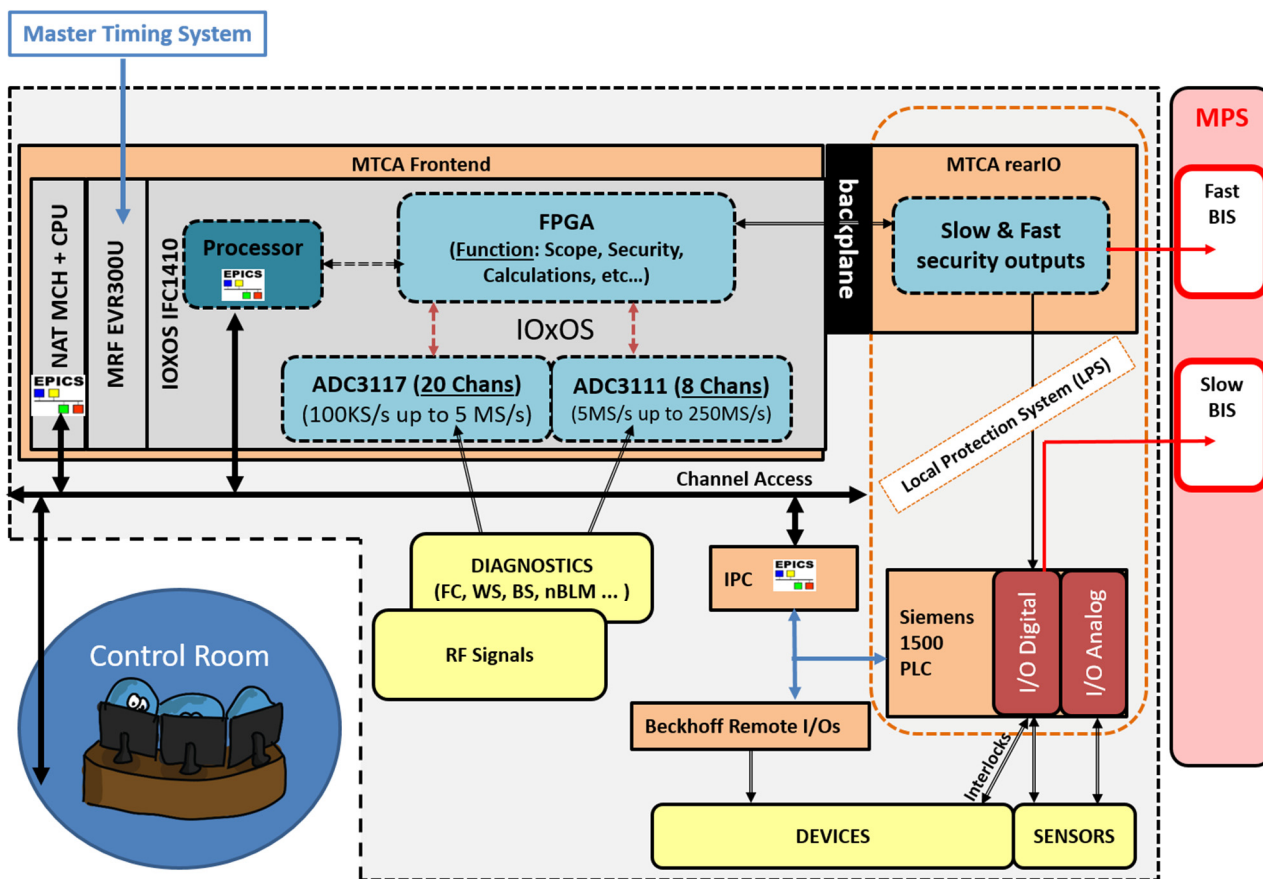


Figure 1: IRFU standard platform.

This set of 2 cards is the core of the standard solution for all our MTCA crates.

IOxOS Fast Acquisition Boards

These last years on VME we have been using the IOxOS FMC boards, which have given us entire satisfaction.

Therefore, we follow the strategy proposed by IOxOS. From the CPU point of view, we replace the VME CPU IOxOS IFC1210 by the MTCA.4 IFC1410 intelligent FMC carrier in AMC form factor featuring an NXP QorIQ T series Power PC processor and one Xilinx Kintex UltraScale FPGA accessible by the user. This AMC IFC1410 is able to carry 2 FMCs and consequently offers a convenient flexibility.

We keep the same FMC acquisition board as used on VME, the fast board ADC-3111 including 8 channels with 16-bit/250MSPs ADCs. See Figure 2.

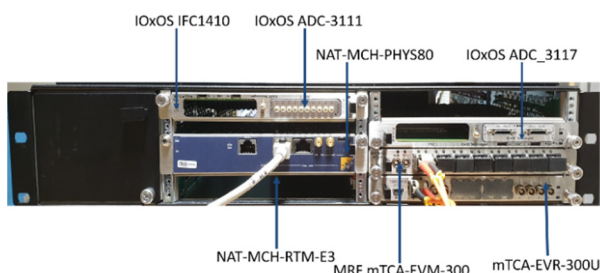


Figure 2: IRFU MTCA platform.

Example with IOxOS nBLM Acquisition

The IFC1410 and FMC ADC-3111 have been successfully used on the Saclay neutron sensitive Beam Loss Monitor test stand [8] for more than one year.

This new detector is based on the Micromegas detector principle that is a gaseous detector with a gas chamber. These nBLMs are designed by CEA for ESS.

As the timing response of this detector is very fast and the duration of a neutron peak is in the order of 100-150 ns, the sampling frequency 250 M Samples per second of the FMC ADC-3111 is used and necessary. This set AMC IFC1410 and FMC ADC-3111, which we have been using for several months, is perfectly adapted and will be integrated again for other nBLM use. In addition to this fast acquisition, the nBLM needs a slow control for the high and low voltage power supplies and a PLC to control the gas.

IOxOS Semi-fast Acquisition

To this configuration, we also add the FMC ADC-3117 board whose sampling frequency is comprised between 1 and 5 M Samples per second. This board has 20 channels (ADC 16-bit 5MSPs) and 2 channels DAC (16-Bit 1 MSPs) and is carried by the IFC1410.

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μRTM Availability

A μRTM can also be connected to the IFC1410 using the backplane connectors and be used for protection. IOxOS offers a μRTM module RCC_1466 featuring high-speed links (SFP 1-5) and including a slot to plug a mezzanine for specific applications. This mezzanine is used at ESS for the fast beam interlock [7] and is the FBI_1482 one.

Slow control

In addition to the MTCA.4 platform, the usual solutions of the slow control are still being used. Siemens PLC 1500 series controls vacuum, cryogenics and interlocks. A Kontron 2U Industrial PC is implemented to run EPICS IOCs dedicated to the PLCs and independent networks.

Beckhoff modules are used for remote inputs and outputs.

TIMING SYSTEM

Purpose

The timing signals are used for the synchronization of the different subsystems of the machine. It is needed to trigger at different locations at exactly the same time and to generate events in sequence with predefined time intervals.

Another major purpose is the timestamping of the events at different locations for the analysis of data, post-mortem-data for instance.

The communication of the MRF signals through the backplane allows to avoid many wire connection problems and results in more reliability.

Solutions

For several years we have been using VME MRF modules on the Saclay ESS RF test stands and IPHI accelerator. For MTCA.4 the timing system modules are currently the MRF mTCA-EVM-300 used as Event Generator (or Master) and the MRF mTCA-EVR-300U as Event Receiver. In addition to being an Event Generator the mTCA-EVM-300 module can also be used as a fan-out or as a concentrator.

The events are generated by the event generator (EVG). Then they are distributed to the subsystems on the event receivers (EVRs) through an optical fibre network in a tree structure. This tree starts from the EVG, is fanned out by the fan-out and achieves the EVRs.

Process

The EVG generates a bitstream including the events, data and clocks on the optical fibre network up to the first fanout that broadcasts on the other fanouts and EVRs and so on. The EVRs receive the events, data and clocks, decode them and execute the orders.

The information regarding the beam is synchronized and includes the beam destination and mode, the required current, the pulse length and other data to be defined.

The timing information is converted to 8-bit event codes and distributed to EVRs as an optical signal. The event clock rate determines the timing resolution (50MHz, 20ns) to (125 MHz, 8ns). The 8-bit distributed bus, independent

of timing events, allows the distribution of eight signals updated with the event clock rate.

The NAT Rear Transition Module CPU NAT-MCH-RTM-COMex-E3 runs the EPICS IOC dedicated to the MRF timing system in each MTCA.4 crate.

The EVRs are also capable of sending event codes up to the EVG that can redistribute the event again, downwards to all the EVRs. We have not yet evaluated this powerful possibility.

SARAF MEBT CONTROL SYSTEM

This standardized platform will be used in the coming months for the control of the source, the LEBT, the MEBT and the Super Conducting Linac (SCL) of the SARAF project. The SCL includes 4 cryomodules. The first two host 13 Low-Beta HWR and 12 superconducting Solenoid Packages (SP). The last two host 14 High-Beta HWR and 8 SP. Here only the MEBT control is described. See Figure 3.

Requirements

The control of the SARAF MEBT requires control of CAENels power supplies for 8 quadrupoles and eight steerers, vacuum and water cooling, 3 rebunchers including 3 LLRF and diagnostics. For Faraday Cups, Profilers or ACCTs the FMC ADC-3117 has the adequate sampling frequency.

Implementation

For the vacuum and water cooling instrumentation, a Siemens 1500 PLC is used. The control of the CAENels power supplies will be based on the EPICS streamdevice and Tcp/Ip communication. The diagnostics Faraday cup, 2 ACCTs and 5 profilers will be controlled from the MTCA.4 standardized platform.

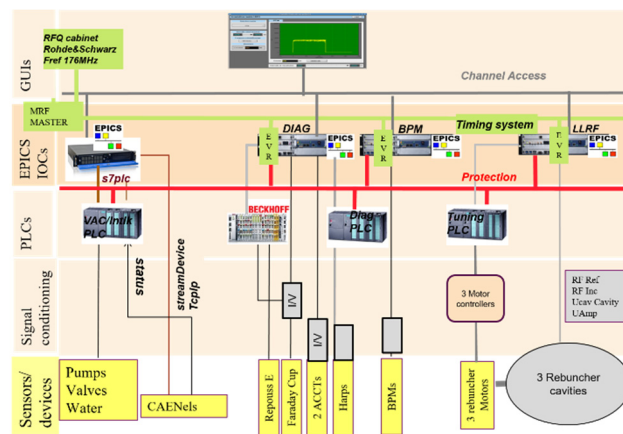


Figure 3: SARAF MEBT synoptic with MTCA crates.

The SARAF LLRF is outsourced for the whole project. The LLRF will rely on an AMC board in charge of the LLRF itself. This AMC will be MTCA.4 integrated with the MRF mtca-EVR-300U and the NAT boards of the platform. The BPMs are also outsourced with the same philosophy of architecture.

CONCLUSION

Even if sometimes we have to struggle with some difficulties linked to new boards and technologies, we are very confident. Furthermore, the good relationship with the ESS team and the proximity of the solutions (MTCA .4, MRF timing system, IOxOS boards) and their support is a real advantage for our small Laboratory.

The installation of the Injector and LEBT control at Soreq will take place in Q1 2020. The MEBT controls should be installed in Q3.

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