ISBN: 978-3-95450-209-7 ISSN: 2226-0358 doi:10.18429/JACoW-ICALEPCS2019-THAPP05

OVERVIEW OF ACQUISITION AND CONTROL ELECTRONICS AND CONCEPTS FOR EXPERIMENTS AND BEAM TRANSPORT AT THE EUROPEAN XFEL

P. Gessler†, H. Ali, F. Babies, K.-E. Ballak, H. Bamaga, B. Baranasic, O. Bieler, N. Coppola, K. Dornack, J. Eilers, D. Emes, B. Fernandes, M. Fobian, T. Freyermuth, S. T. Huynh, N. Jardón Bueno, M. Meyer, O. Oshtuk, P. Parlicki, J. Reifschläger, S. Sayar, H. Sotoudi Namin, M. Stupar, J. Tolkiehn, H. Vega Pérez, S. Wagner, J. Zach
European X-Ray Free-Electron Laser Facility, Schenefeld, Germany

Abstract

FPGA based fast electronics to acquire and pre-process signals of detectors and diagnostics and PLC based hardware and software for motion, vacuum and other control and monitoring applications are key elements of the European X-Ray Free Electron Laser. In order to bring the newly developed scientific user facility up and running, the underlying electrical and electronic components require a diverse array of tools and processes to be developed in order to meet the continually adapting requirements and make use of technological advances. Many challenges were faced, including high availability and up-time, adaptability to a dynamic environment, rapid lead-time for integration of complex components, numerous instrumentation installations and commissioning, high time resolution and subsequently, high demands on data and sampling rates, synchronization and real-time processing. In this contribution we will provide an overview of the selected technologies, developed concepts and solutions along with generically designed frameworks and tools, which aim to provide a high degree of standardization on the control systems and even automatic generation from requirements to final install.

INTRODUCTION

The European X-Ray Free-Electron Laser Facility (EuXFEL) is located in northern Germany with a length of about 3.4 km. It provides coherent x-ray pulses between 260 eV and 24 keV and a duration of less than 100 fs at three beamlines. At present, six instruments are located at the end of the beamlines, which provide a wide span of environments and instrumentation to allow scientific research in many fields [1].

Due to the underlying super conducting accelerator technology, the time structure of the photon pulses delivery is organized in short bursts (also called trains) of up to 600 µs every 100 ms. In these bursts up to 2700 pulses could be generated and directed to up to three of the six instruments at a time. The minimal spacing between pulses is 220 ns and therefore equivalent to a repetition rate of 4.5 MHz. These parameters are of relevance for the design of the electronics and acquisition system since high-resolution measurement during the bursts is often required, and in the gaps between the bursts, time for data processing and transfer is available.

A significant number of equipments are required and have to be accurately remotely or automatically operated. These could be categorized as follows: (1) slow control and monitoring elements like vacuum systems, positioning, temperature control, etc., and (2) fast diagnostics and detectors. While the first category includes a very large number of individual channels of sensors, and actuators, which require only moderate time resolution of seconds to sub-ms range, the second category demands a high sampling rate (in the order of multiple GHz) and high data bandwidth (in the order of 10 GBytes/s on a single detector). On such speeds and band widths, the pre-processing of acquired signals is an important aspect in order to implement data reduction and to reduce the latency in the system to process and react on the measurement signals in real-time.

The mentioned aspects are important boundary conditions and significantly impacted the selection and development of the underlying electronics for control and acquisition. It should be mentioned here, that there is a split of responsibility for the accelerator part up to the undulators on one side and the photon beam transport and experiment stations on the other side. This work only focuses on the later part. Information about the accelerator and undulator related control electronics could be found, for example in [2].

VISION AND APPROACH

In the planning phase about 130 individual components were counted, where each one could be relatively simple in terms of control, like an imager with one motor and related position switches to insert a screen, digital outputs to control equipment powering and to enable or disable a LED for testing purposes. But one component could also be an x-ray split and delay line with about 100 individual motors and related switches and encoders. Taking a closer look to the quantity of the elements to be controlled, monitored, digitized and processed, one part of the challenge could be easily seen, which is the integration of thousands of individual elements like motors, pumps, valves, gauges, sensors and analogue and digital signals.

In order to master the task not only of how to integrate all these elements into the control system of European XFEL, but also how to be able to support and maintain it

† patrick.gessler@xfel.eu

ISBN: 978-3-95450-209-7 ISSN: 2226-0358 doi:10.18429/JACoW-ICALEPCS2019-THAPP05

in the years to come (including modifications, extensions, etc.), a generic and modular solution had to be found and developed. Key aspects of the envisioned system and solutions were:

- Allow to connect from equipment up to final visualization in terms of naming, identification, documentation, tracking, and functionality
- Allow for real-time and deterministic interaction of critical aspects across all control equipment
- Maximize re-usability and provide a homogeneous environment
- Minimize manual interventions through automated processes and interfaces in the integration process and thus reducing time and errors
- Develop and provide key set of generic solutions to cover almost all applications (frameworks, common hardware platforms, generic elements)

Even with a set of standardized solutions, there is still the challenge of the actual design, production, testing, installation and commissioning of the required electronics. That implies, that not only the technical concepts and solutions had to be identified and developed, but also processes, related staffing and contracts for the design, production, installation, commissioning and quality control had to be developed and implemented.

SELECTED TECHNOLOGIES AND TOOLS

Industrial Standard PLC Systems

As a key ingredient for robust and long life-time slow control and automation solution a Programmable Logic Controller (PLC) based implementation was selected. In our case the EtherCAT bus terminals and PLC family from Beckhoff [3] were chosen. Some important decision driving factors were the modern Ethernet based real-time and open standard EtherCAT fieldbus, a strong support of motion systems, and support of multiple PLCs on one CPU. The TwinCAT 3 programming environment supports IEC61131-3 and object oriented programming, which is an important aspect for the design concept outlined in the following section. For some special cases also controllers from other vendors are used like PI for Hexapods as well as xyz-nano cubes, Elmo MC and Technosoft for strong and very weak stepper motors, and FESTO for pneumatic islands.

MicroTCA Platform for Fast Electronics

Due to the many decentralized locations, where sensitive measurement signals are detected and timing signals are required, a relatively compact form factor solution suitable for physics applications with high-reliability, redundancy and remote access possibilities was required. Following the developments and choice from the European XFEL machine side at DESY, we also selected the MicroTCA.4 standard. This platform provides high-speed interconnects via PCIe and Ethernet with redundant cooling and power supply as well as full remote monitoring, control and automatic failure detection and reaction. Based on this system we use Field Programmable Gate Array (FPGA) equiped modules (called AMCs), which provide digitization, synchronization, online processing and real-time data rejection (vetoing) capabilities.

Electrical Computer Aided Design (ECAD)

An important aspect of the design, construction, documentation and maintenance of the electrical instrumentation infrastructure is the usage of a suitable electrical CAD program. Besides the design of the PLC systems also the whole cable planning, routing, and documentation as well as the change management to adapt to the evolvement of the instrumentation has to be possible. We selected EPLAN P8 for this task, which fulfills the requirements and also provides powerful interfaces for import and export as well as automation of workflows, which is an important aspect outlined in the next section.

Bug, Feature, Task Tracking and Ticketing System

Besides bug and feature request tracking, typically required for the PLC and FPGA developments, also documentation and tracking of general tasks and a ticketing system was identified to be important for development as well as the construction, operation, maintenance and support of the infrastructure. The web based Easy Redmine [4] was selected for this purpose, which is also used by many other groups within European XFEL.

Source Code Versioning Repository

Historically, the selected version tool for PLC and FPGA developments was subversion (SVN) [5]. Besides the basic functionality and tolerance for binary files it also provides a good integration with Redmine. However, except for some cases, we migrated the repositories to GitLab [6], since it provides a significant advantage related to code review and continuous integration workflows.

Online Monitoring and Alarm System

In order to provide a high availability, prompt service and maintenance as well as to identify possible issues as early as possible, we are using Nagios [7] as a professional monitoring and alarm tool. This covers all PLC systems and related infrastructure like cooling and power supplies as well as the MicroTCA systems. Besides this rsyslog is used to centrally monitor the operating system (OS) of the MicroTCA CPUs.

Automatic OS Installation and Configuration

A typical task is the installation, update and (re-) configuration of the operating system. In our case this was and is required for 35 Linux based MicroTCA CPUs for the scientific instruments and photon beamlines in the tunnels. In order to simplify this activity and ensure conformity of the different installations we recently adopted the Puppet tool [8] in combination with Foreman [9]. Puppet profiles definition include users and groups rights access, packages, drivers as well as system tools, guaranteeing that all

ISBN: 978-3-95450-209-7 ISSN: 2226-0358 doi:10.18429/JACoW-ICALEPCS2019-THAPP05

systems have the same environment. Profiles are defined according to CPU's manufacturer and architecture and its usage e.g. production, development or testing.

DEVELOPED CONCEPTS AND SOLUTIONS

PLC Systems and Related Infrastructure and Interfaces

Due to the vast number of equipment required to be integrated for control or monitoring, different boundary conditions had to be observed and suitable concepts and solutions had to be developed.

Mechanical and Electrical Design All PLC related electronics had to be placed in 19 inch industrial racks, placed in rack rooms above the scientific instruments. Due to radiation protection, the actual instruments are located in shielded hutches below the rack rooms and signal cables between PLC systems and the equipment at the beamline had to be routed through chicanes. Typical lengths of cables are between 20 and 40 meters. On the cable paths many cables share the same cable tray which makes shielding an important aspect.

As a key concept a strong standardization, modularization and interfacing of the PLC environment was followed on all architectural levels (e.g. mechanics, electronics and software). In order to achieve a high-density of PLC terminals within the 19 inch and about 80 cm usable depth racks, while maintaining modularity and clean interface to the cabling, a mechanical form-factor was designed as shown in Fig. 1. It consists of a mechanical 19 inch, 5U high and about 50 cm deep frame, where two removable modules could be inserted, which include the PLC terminals, EtherCAT couplers and specific fusing. The back side of the modules include modular connectors [10] (wired to the inner PLC terminals), which mate with the counter connectors, which are mounted on the back of the frame and are part of the cabling. In that way a decoupling of the cable production and installation and the PLC module production and installation is achieved. Also removing of modules for maintenance or modification during the lifetime of the systems is easily possible without manual disconnection of installed cables.

Intentionally, power supplies, cooling and PLC CPUs are not included in the PLC modules. Each rack with PLC modules host two 1U high chassis for hot-swappable power modules [11] to provide 24 V and 48 V resp. This solution allows for a very high density of power (up to 8 kW in 1U) as well as redundancy and remote monitoring. Fan units with alarm signals and air ducts ensure reliable airflow within the racks. The PLC CPUs are concentrated in each rack room for the resp. instrument or the so called balcony rooms for the resp. tunnels. Each of the scientific instruments require about 10 to 18 of these special industrial computers to implement the PLC infrastructure. They are also powered by 24 V through the previously described power supply solution. However, besides redundant number of power modules, also two redundant primary power lines (from two providers) are used to minimize the risk of power failures.

Figure 1: Image of the mechanical 19 inch frame with two PLC modules. The right module is only half-way inserted and allows to see the Harting Han series connector frame at the back.

Each PLC CPU communicates with the respective PLC modules via a redundant EtherCAT cable connection (loop) in order to be tolerant against single module failures or to allow removing of single or consecutive modules for service tasks. In order to allow also interactions between PLCs a cross-PLC / loop communication through EtherCAT bridges is implemented with an additional hierarchy to also allow interaction between instrument and tunnel PLC systems (as often required for vacuum control related tasks) and even between beamlines.

PLC Software Design Also the PLC software architecture is following a modular and clear interface approach. For each type of equipment (with a specific hardware interface documented in an EPLAN macro) a corresponding object class called softdevice was developed. Each softdevice implements all required low-level features to operate the resp. equipment. The softdevices are part of the developed PLC framework, which also includes communication interfaces between softdevices and between the PLC and the Supervisory Control and Data Acquisition (SCADA) system, which is on our case Karabo [12], which was developed and is provided by the European XFEL Controls group. The PLC framework is organized as a versioned library to ensure clear identification in running systems, conformity of interfaces and upgrade procedures. Each PLC requires a project, which includes the framework library and instantiates all required softdevice classes and their default parameters for each connected equipment. Furthermore, automatic interaction between softdevice instances are defined in the project, which are (currently) only implemented as interlocks to reduce the risk of damages of the instrumentation.

ISBN: 978-3-95450-209-7 ISSN: 2226-0358 doi:10.18429/JACoW-ICALEPCS2019-THAPP05

Automatic PLC Project Generation Not only the developed solutions are required in order to adapt to the boundary conditions, also the procedure to prepare the projects for the required PLC systems had to be developed to accomplish the significant amount of work with a limited number of experts and to allow the further maintenance, extensions and modifications while maintaining full and consistent documentation. For this reason the PLC Management System (PLCMS) [13] was developed, which generates PLC projects based on the EPLAN documentation, information of the PLC framework and to implement interlock functionality based on user defined conditions and actions documented in Excel spread sheets. With that approach, the work load was significantly reduced, the consistency between ECAD designs, hardware and PLC projects ensured and more transparency provided. A further aspect of the transparency is implemented in the PLC framework, which provides, on-connect from the control system, a complete self description of all instances of softdevices, their names and available parameters and access levels. During run time a special monitoring device provides all important information about the PLC system. Besides the control system interface also the Nagios system is interfaced to each PLC and informs about any issues related to the PLC software or hardware status.

PLC Security As PLC systems are a critical part of the whole European XFEL, also security is an important aspect. Besides the developed interface to the control system, many potentially insecure additional interfaces via the network interface (AFS, OS specific services, Nagios monitoring, NTP, etc.) are accessible. Therefore we implemented a strictly isolated network approach. All PLCs of one instrument or tunnel reside in an own private network. To that network a small number of server machines are connected with a second network port, which is not routed to the outside. These servers host the control system (Karabo) devices, which provide the only interface to the facility for normal operation. Additionally, there are two or three virtual support machines running on the servers, which are required to service the PLC systems. All these servers and machines are password protected and only accessible by the required expert personnel. The interface between Karabo and a PLC allows only a single connection and thus guaranties exclusive access. Although the PLC defines access levels for each accessible parameter, authentication and user access right management is not part of the PLC system and has to be provided through the control system.

MicroTCA Based Solutions

Timing System A crucial element in acquisition electronics at an x-ray free-electron laser is the so called timing system. It has to provide accurate and stable triggers to synchronize acquisition, provide reference frequencies (clocks) to align sampling rates and other sequencing clocks in frequency and phase as well as to distribute pulse pattern information and other parameters in a deterministic way. The European XFEL Timing System was a development between DESY and Stockholm University [14,15] and is implemented as an AMC called X2Timer. We developed two standard adapter boxes, one to convert LVDS (Low-Voltage Differential Signaling) trigger and clock outputs of the AMC into TTL (Transistor-Transistor Logic), and one in the opposite direction for special interlock inputs of the AMC.

Digitization of Analogue Signals Besides timing, the most common applications where the MicroTCA platform is utilized, are AMCs to digitize analogue signals from detectors (e.g. (avalanche) photo diodes, diamond plates, multi-channel plates). Depending on the relevant properties of the transient signals (e.g. energy of a pulse, peak time of a pulse, shape of the signal) different signal shaping, sampling rates, resolution and processing requirements have to be maintained or provided. Based on an initial requirements survey, three different classes of digitizers were identified: (1) sampling rate of about 100 – 200 MSPS (Mega samples per second) for known pulse shape and interest in only energy of pulses or a generally relatively slow signal shape; (2) sampling at about 2 GSPS (Giga samples per second) to also allow for peak time detection of fast pulses and spectral information of moderate time-of-flight signals; and (3) sampling of 10 GSPS and more usually for time-of-flight signals with high resolution.

For the first class the SIS8300 from Struck Innovative Systems [16] was selected, which provides 10 channels of up to 125 MSPS with 16 bit nominal resolution. A special rear-transition module (RTM) was developed, which allows to stretch the analogue signal before it is digitized and therefore also allows to process pulses shorter than the sampling rate. The AMC also includes an FPGA as central element, which is equipped with an in-house developed firmware including an energy detection algorithm.

For the second class, intensive market research and discussions with possible vendors lead to a newly developed product by Teledyne SP Devices [17], called ADQ412-4G-MTCA. This AMC provides 4 channels with up to 2 GSPS or 2 channels with up to 4 GSPS (software configurable) at 12 bit resolution. The powerful FPGA on the AMC includes a closed source based firmware and a user space, where signal processing and data handling can be implemented.

For the third class, only during the last two years first products reached the commercial market. In our case, we started to integrate and port developments to the new generation of Teledyne SP Devices ADQ7 modules, which provide up to 10 GSPS with 14 bit resolution. However, faster sampling solutions (e.g. 56 GSPS at 8 bit) are still very expensive and related processing difficult and therefore their integration has not started yet.

FPGA Based Systems

Separation into Board and Application FPGA projects at the European XFEL are developed in VHDL (Very High Speed Integrated Circuit Hardware Description Language). The top level design is separated into two

ISBN: 978-3-95450-209-7 ISSN: 2226-0358 doi:10.18429/JACoW-ICALEPCS2019-THAPP05

specific modules: Board and Application. The Board module includes all code related and specific to monitor and configure board features and also provides the related interfaces (e.g. for ADC/DAC, DDR2 controller, Clocks, etc.) to the Application module. User algorithms and applications are implemented in the Application module, which may be board specific. A basic Input / Output (I/O) board interface is provided on the Application module so that users focus only on the development of their application. Improvements and further development on the board interfaces is performed by expert designers while not interfering with developments on the Application module. This fixed structure allows for easy porting and update on both board and application code. It provides an environment for firmware programming for standardized and future hardware.

Automated Register and Memory Generation User registers and memories are defined using an in-house further developed version of the Internal Interface (II) bus [18]. The Internal Interface is a bus protocol and defined in an VHDL package and consists of a set of VHDL functions with an API that eases register definition and access. Register properties are collected in an VHDL table, which can be defined per module, and includes access rights, data type (unsigned, signed, bool), bit size, number of integer and fractional bits, memory length and a brief description. The registers and memories are accessed via PCIe or Ethernet devices. Assignment of address is performed at the hardware level during the compilation process. After compilation, an XML file with all register information, including the assigned addresses, is available. The interfacing software library used in the European XFEL control system is able to interpret this file and provides a user friendly environment which allows users to communicate with the design on the FPGA.

Standard Register Set and SHAPI In order to allow a universal identification of the installed hardware and firmware, we developed a standard register set concept, which is a predefined set of registers starting at address 0 and with a pointer to the next standard register set in the address space. In these registers crucial information about the type of hardware, functionality and versions is available even without access to the previously described XML files. This concept was further developed with different institutes and industry within a working group in PICMG (PCI Industrial Computer Manufacturers Group) and was released as Standard Harware API (SHAPI) as guide lines [19].

Graphical Programming and Simulation While using graphical programming languages is a suitable approach to FPGA development, some of the more demanding and specific modules require a certain level of HDL knowledge to be properly implemented and maintained. For application development the environment provided by graphical tools is more intuitive and easier to develop for users interested in implementing their algorithms on an FPGA. Preference over HDL wrappers is based on users having to learn and familiarize with a programming language, its syntax and coding methodology, which may take a considerable amount of time. Special attention is also given to simulation of algorithms. HDL based simulations usually do not provide an easy integration of external data as well as functions for signal analysis and visualization (e.g. histograms). An environment where users can test their FPGA algorithm with real experimental data and obtain relevant results is highly beneficial. Taking these points into account, a high level FPGA framework based on the MathWorks Simulink tool is being developed at the European XFEL, that allows for users to develop their algorithm modules. Our Board/Application structure allows for FPGA experts to use HDLs to implement and improve board features without interfering with the application development. Users of our FPGA framework can use the modules available on the Simulink Library to focus on their algorithm implementation. From the FPGA project point of view, Simulink based designs are applications with their own memory in the bus protocol address space. The framework also includes the standard registers of the II bus, so modules defined in this environment will interface the control system in the same manner. In addition, algorithms developed in VHDL can also be added to the Simulink environment.

Special Algorithms for Digitized Signals FPGA algorithms are already in place for processing of digitizer data on the hardware. This data is provided together with the raw data, allowing further systems to take faster decisions not only concerning the quality of the data but also for diagnostics and status of the beam. Algorithms include peak integration, peak (time) detection and zero suppression.

Pulse Train Information Available on all FPGAs Information concerning train pulses is available to all devices that are able to receive the timing information, this includes the digitizers on the MicroTCA platforms, before the train arrives. As such, this information could be used to filter generated data according to a specification given by the user. In addition, fast processing devices (FPGA based ones for example) provide algorithm results that could be used to determine the quality or relevance of the data.

Real-Time Data Rejection via VETO System The VETO system is a device that is able to combine these different data sets and take a decision, per pulse and according to the user criteria, on the data. Data would be classified as Golden, Non-VETO (e.g. uncertain) and VETO, which would mean save, save if possible and do not save respectively. These decisions can be forward to our Detectors with a latency of only some microseconds and stored in the European XFEL DAQ system.

WORKFLOW FROM REQUIREMENTS TO RUNNING SYSTEMS

Based on the previously described concepts and solutions, this section will briefly outline the typical workflow starting with a requirement for a specific instrumentation up to the running system.

ISBN: 978-3-95450-209-7 ISSN: 2226-0358 doi:10.18429/JACoW-ICALEPCS2019-THAPP05

The usual starting point is the need from a scientific group to integrate a new instrumentation beamline component like a diagnostic imager. The person will fill in a Component Requirement Document (CRD) form, which includes a detailed list of all equipment involved, timing requirements, and many other information. This document is often discussed before handing it in with electronics and software experts to clarify general questions. Afterwards it will be processed by different experts of PLCs, timing, digitization, cabling and control system until it is formally approved. Afterwards a designer will create required EPLAN documentation, which is reviewed and checked before it is sent to production (if PLC modules are involved). Additionally the design is integrated into the overall instrument integration project documentation, which includes the PLC loop structure, locations as well as all required cabling. The responsible cable planner will add further cable length, path and connection box information to the design before the cable production is triggered (in-house or by external company). Also based on the integration project the full PLC loop information is exported as XML files. Based on the designs the infrastructure in the involved racks is prepared (e.g. power supplies, cooling, frames, etc.) to allow the following installation of cables and PLC modules. Also the PLC projects are generated based on the exported XML file(s). Once all produced elements are ready and acceptance tested, the installation, deployment and initial test are carried out jointly with the requesting group and the controls group. Possible issues are resolved and the system handed over to the requester for technical commissioning and operation. From then onward only support activities and work based on change request are carried out in agreement with the operating group.

EXPERIENCE IN THE OPERATION

Up to now, we are operating about 120 PLC systems and a sum of about 8.500 terminals in more than 500 PLC modules. The about 10.000 softdevices include 2200 motors, 800 vacuum pumps, 1500 digital or analogue outputs, 4000 digital or analogue inputs, and many special devices more. Besides the PLCs, there are 35 MicroTCA systems in operation. In order to provide prompt support we do not only react on issues of the alarm system and support request tickets, but also provide 24/7 on-call duty (OCD). In average, we receive about five OCD calls per month outside of the usual office hours. If we exclude cases, where the cause of the issue was outside of our systems (e.g. sensor/actuator issues, control system issues), there are three main causes identified: (1) insufficiently commissioned systems, mostly very recently commissioned and not correctly parameterized; (2) undesired changes of cabling during recent shutdown work, where cables were disconnected and not correctly reattached or other kind of side effects, which were only realized during following usage; (3) undetected change of parameters during maintenance or updates.

FUTURE WORK

It has to be stated clearly, that the main goal for the PLC system development, production and installations was to manage the integration of the very large number of equipment at all with the available time and persons for the installation and commissioning phase of the European XFEL and provide basic control and monitoring capabilities as well as interlock capabilities to reduce the risk of hardware damages and thus downtime and costs. As a consequence, the capabilities of the used PLC technologies are only exploited in a limited way. For example powerful automation functionalities (beyond interlocks) are not yet provided, nor are control loops (except for motion control and other limited cases). This will be the future focus combined with related PLC framework developments. Furthermore, the field of machine safety in terms of IEC61508 is currently a field of development. So far we only integrated equipment, where no person safety relevant functionality and safety integrity level were required by the manufacturers of the related components. This is currently changing for some new components. Therefore safety PLC integration into the PLC infrastructure is currently investigated and worked on. Finally, the (future) needs of the scientific groups as well as the technological developments are observed in order to drive investigations and developments for the future in order to be able to support latest technology detection, control, online-processing and communication methods.

ACKNOWLEDGEMENTS

The described technologies and developed solutions are only one part of the overall installations and efforts in order to allow the operation of the European XFEL. This was only possible with strong collaboration between many groups and partners. Therefore we would like to thank all our colleagues of the various groups at the European XFEL for their active support and collaboration during the development, installation and commissioning as well as for their patience and adjustment of expectations. We also would like to thank the DESY MCS group for very good collaboration related to the MicroTCA and timing system. Finally, we want to thank the Electronics and Detection Systems Division at NCBJ in Poland for their input, strong support and long-term collaboration in the PLC module production.

REFERENCES

[1] T. Tschentscher, *et al.* “Photon Beam Transport and Scientific Instruments at the European XFEL”, *Applied Sciences*, vol. 7, Iss. 6, p. 592, Jun. 2017, doi.org/10.3390/app7060592

[2] T. Wilksen *et al.*, “The control system for the linear accelerator at the European XFEL - status and first experiences”, in *Proc. 16th Int. Conf.* on *Accelerator and Large Experimental Physics Control System (ICALEPCS’17)*, Barcelona, Spain, Oct. 2017, pp. 1-5, paper MOAPL01.

[3] Beckhoff Automation GmbH & Co. KG, https://www.beckhoff.de/

ISBN: 978-3-95450-209-7 ISSN: 2226-0358 doi:10.18429/JACoW-ICALEPCS2019-THAPP05

[4] Easy Redmine, https://www.easyredmine.com/

[5] Subversion, https://subversion.apache.org/

[6] GitLab, https://gitlab.com

[7] Nagios, https://www.nagios.org

[8] Puppet, https://puppet.com/

[9] Foreman, https://theforeman.org/

[10] Harting Industrial Connectors Han Series, https://www.harting.com/US/en/solutions/industrial-connectors-han

[11] TDK Lambda HFE1600 Series, https://www.us.tdk-lambda.com/lp/products/hfe-series.htm

[12] S. Hauf, *et al.*, "The Karabo distributed control system", *J. Synchrotron Radiat.*, vol. 26, part. 5, p. 1448-1461, Sep. 2019, doi.org/10.1107/S1600577519006696

[13] S. T. Huynh *et al.*, "Automatic Generation of PLC Projects Using Standardized Components and Data Models", presented at the 17th Int. Conf. on Accelerator and Large Experimental Physics Control Systems (ICALEPCS'19), New York, NY, USA, Oct. 2019, paper THAPP01, this conference.

[14] A. Hidvegi *et al.*,"Timing and triggering system for the European XFEL project - a double sized AMC board", in *Proc. 18th IEEE-NPSS Real Time Conference*, Berkeley, CA, USA, June 2012, doi:10.1109/RTC.2012.6418093

[15] P. Gessler, "Synchronization and Sequencing of Data Acquisition and Control Electronics at the European X-Ray Free Electron Laser", Ph.D thesis, High Freq. Dep., University of Technology Hamburg-Harburg, Hamburg, Germany, 2015, doi:10.3204/DESY-THESIS-2015-049

[16] Struck Innovative Systeme, SIS8300 µTCA for Physics Digitizer, https://www.struck.de/sis8300.html

[17] Teledyne SP Devices, https://www.spdevices.com/

[18] K. Pozniak, "Internal interface, I/O communication with FPGA circuits and hardware description standard for applications in HEP and FEL electronics ver. 1.0", DESY, Hamburg, Germany, DESY-TESLA-2005-22, 2005.

[19] Standard Hardware API, PICMG, https://www.picmg.org/wp-content/uploads/PICMG_MTCA_DG_1-Standard_Hardware_API_Design_Guide_RELEASED-2017-01-09-002.pdf