THE ITk COMMON MONITORING AND INTERLOCK SYSTEM

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Abstract

For the upgrade of the Large Hadron Collider (LHC) to the High-Luminosity Large Hadron Collider (HL-LHC) the ATLAS detector will install a new Inner Tracker (ITk), which consists completely of silicon detectors. The most inner part is composed of pixel detectors, the outer part of strip detector elements. All together ca. 28000 detector modules will be installed in the ITk volume. Although different technologies were chosen for the inner and outer part, both detectors share a lot of commonalities concerning their requirements. These are operation in the harsh radiation environment, the restricted space for services, and the high power density, which requires a very efficient cooling system. While the sub-detectors have chosen different strategies to reduce their powering services, they share the same CO_2 cooling system. The main risks for operation are heat ups and condensation, therefore a common detector control system is under development. It provides a detailed monitoring of the temperature, the radiation and the humidity in the tracker volume. Additionally, an interlock system, a hardware based safety system, is designed to protect the sensitive detector elements against upcoming risks. Another constraint is that - once the detector is installed - its components are not accessible for several years or even for the lifetime of the detector. Thus the control system must be fault tolerant and provide very good remote diagnostics. The components of the ITk common monitoring and interlock system are presented.

INTRODUCTION

In the third long shutdown of the LHC, when it will be upgraded to the high-luminosity LHC, the ATLAS experiment will install a new tracker. It consists of the pixel detector at small radius close to the beam pipe and a large area strip detector surrounding it [1], [2]. Although the segmentation of the sensor cells will be different for the pixel and strip detector, the ITk will be an all silicon detector.

Therefore, the design of the tracker is driven by major common requirements. Main constraints for the construction of the detectors and their control systems are the high power density, the harsh radiation environment and the low material budget requirement inside the tracker volume.

Pixel and strip detector modules are composed of the sensor and the related front end electronics. In total there

are about 10000 pixel detector modules with 6 billion channels covering an area of ca. 13 m^2. The strip detector consists of roughly 18000 modules with 60 million electronic channels and covers an active silicon area of 165 m^2. These large number of readout channels cause the high power density inside the tracker volume. The modules are mounted on different carrier structures. These are staves in the barrel region, while rings and disks carry the modules of the endcaps. Thin cooling pipes are integrated into all carrier structures.

To handle the low material budget requirement the sub-detectors developed different strategies to reduce the volume of the power cables. The strip detector makes use of local DC-DC converters, while the pixel detector powers a group of up to fourteen detector modules in a serial chain. Further both sub-detectors foresee local monitoring chips, which reduce the number of sense lines. Due to the different powering schemes, the requirement concerning the Detector Control System (DCS) are also detector specific. This leads to different DCS Application Specific Integrated Circuits (ASIC). In case of the strip detector all DCS information is sent through data path, while in case of the pixel detector part of the data is sent through the normal data path, but some monitoring data is sent out through an independent path. Challenge for all ASICs is the radiation hardness.

Besides the sub-detector specific ASICs it was decided to search for common DCS tools where possible to reduce the development efforts and to simplify the operation and the long term maintenance. This is the subject of this article.

COOLING SYSTEM

Due to the highly power dissipation of the detector modules a high efficient cooling system is required. The cooling system will be based on evaporating CO_2 [1], using the 2-Phase Accumulator Controlled Loop cooling concept [3]. There will be a common cooling system for strip and pixel detector, which will be made up of several interchangeable cooling plants. Such a system does not require any active components inside the detector, just temperature sensing of the cooling pipes is needed. CO_2 was chosen for its significant mass savings inside the detector volume. Furthermore, CO_2 is radiation hard, cheap in use and environmentally friendly. The evaporation temperature is driven by the needs of the pixel detector. To ensure a thermal stability over the full operational lifetime, the coolant

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must be delivered at the inlets of the detector at -35 °C. The overall power estimate for the cooling plants is ca 200 kW.

Following the CERN wide strategy, the operation of such a complex system is left to the experts. The risk is too high that an unexperienced shifter causes problems by hasty actions. This clear separation is realized by separated networks for ATLAS DCS and the CO_2 Cooling System (CCS), which is connected to the technical network of CERN. While any changes of the operational parameters are left to the cooling experts, monitoring data is exchanged between CCS and ATLAS DCS via the Data Interchange Protocol (DIP) [4]. A DIP server allows for publishing of data and subscribing to data of interest. This data exchange includes summarizing data, which is relevant for ITk, and the temperature monitoring of the cooling pipes. This information is collected by ITk DCS and published for CCS, which needs this data for debugging and tuning of the cooling system, see below. As this data exchange relies on several components to be up and running, a complementary data transfer based on ModBus is foreseen, as a type of data tunneling. This transfer is limited to a few most important parameters like the status of the cooling plants or the set temperature. In case of severe problems there is an additional hardware signal per cooling plant, which is fed into the interlock system.

GAS SYSTEM

To ensure a dry operation environment, the gas system flushes the ITk volume and the outer service volume with dry nitrogen.

Like the cooling system the gas system is not part of ATLAS DCS but belongs to the technical network. This means that all control is performed by the "gas" group, while ITk is provided with monitoring data (e.g. gas flow, pressure) via DIP. To ensure the safety the same strategy as for the cooling system is used. In case of malfunctioning there is a hardware signal available which will be routed into the interlock system.

ELMB2

The Embedded Local Monitoring Board (ELMB) was originally developed by the ATLAS DCS group as a multipurpose, low cost data acquisition and control device. As this concept has proven to be very successful, it was decided to design a follow-up, the ELMB2 [5].

The ELMB2 is a small plug-in module with a size of a credit card, its building blocks can be seen in Fig. 1. Its local intelligence is provided by a micro-controller. Its main monitoring and control applications are running on it. 64 16-bit multiplexed ADC and 34 digital I/O channels are available. Additional devices such as a Digital Analog Converter (DAC) can be controlled making use of the Serial Peripheral Interface (SPI) bus. Communication with the control station is realized by a Control Area Network (CAN interface) using the CANopen protocol. Irradiation tests have shown that the ELMB2 can stand a total ionizing dose of up to 20 krad.

Another advantage of the ELMB2 is that all firmware, middleware and software tools which are required for integration into the ATLAS DCS already exist.
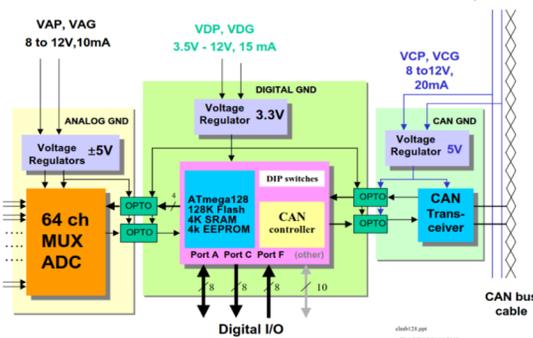

Figure 1: Embedded Local Monitor Board V2 [5].

THE ITk ENVIRONMENTAL MONITORING SYSTEM

Besides the sub-detector specific control elements, as described in the introduction, there is the ITk common DCS, which provides independent data. Figure 2 gives an overview of the ITk common DCS. All sensors must withstand the harsh radiation environment of the tracker, while most of the readout is installed in the counting room, which is a radiation safe area. Please note that the figure concentrates on systems whose sensors are located inside the ITk volume, which are environmental temperature, humidity and radiation monitoring. The sensors are located in all critical points which need supervision. Depending on the location, the requirements concerning accuracy or radiation hardness might vary. Additionally, a small number of vibration and stress sensors are foreseen outside the ITk volume, e.g. on the outer side of the ITk cylinder. These sensors and their related readout will make use of commercial components. The readout will be located in the counting room and therefore also the radiation hardness is not an issue. In the following we concentrate on the systems, where the sensors are installed inside ITk. The distance between the sensors and the counting room is approximately 100 m.

According to the environmental conditions the ITk can be split into three different regions: the strip and pixel detector volumes, and the outer service volume, which encloses the sub-detectors completely.
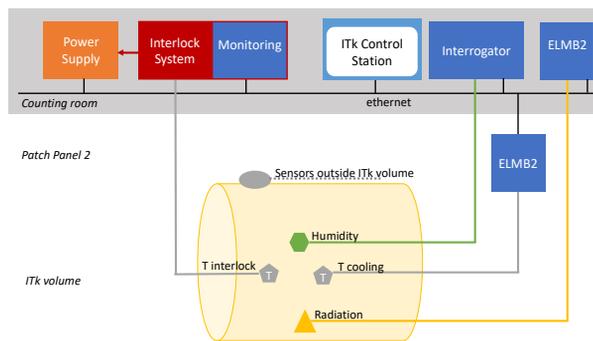

Figure 2: Overview of ITk common DCS.

Temperature Monitoring

The majority of the temperature sensors will be installed on the cooling pipes, ca. 1000 sensors. A smaller part is distributed in the volumes of strip and pixel and the outer service volume. The required accuracy of 0.5 K is driven by the needs of the sensors located on the cooling pipes as this data is required to debug the performance of the cooling system. The temperature sensors (category A) must fulfil the following requirements:

- Accuracy ± 0.5 K
- operation range -45 °C to +20 °C
- radiation hard up to 900 Mrad
- small tolerances corresponding to ± 0.1 K
- long term stability over several years
- operation in magnetic field of 2 T
- extended measuring range (-80 to +200 °C) with reduced accuracy of 2 K
- distance between sensor and readout: 15 m
- low sensitivity against wire resistance

Taking into account the required high radiation hardness it seems that just resistance temperature detectors can be chosen. The needs can be fulfilled by Pt sensors, the choice of a Pt 10 kΩ is dominated by the required low sensitivity against cable resistances. Error estimates have shown that Pt 10 kΩ 0.1% can be used with a two wire readout. Given the limited available space inside the tracker volume, this is the only way to go for the majority of the temperature sensors.

Driven by the demanding requirements of the pixel detector concerning the cooling system, additionally a few sensors, located on some of the pixel cooling pipes, are required with an increased accuracy of ± 0.2 K (category B sensors). This can only be achieved by a four wire readout.

The readout of the Pt sensors is based on the ELMB2. We make use of its 16 bit ADC, which has several input ranges. In order to keep the error due to the ADC input current low, we selected an input range of 100 mV which has an input current of only 100 pA.

To reduce the impact of the cables we try to install the readout as close as possible to the ITk volume. The closest locations, which offer enough space, are the patch panels 2 (PP2) which are still inside the ATLAS detector. The expected dose for this region is below 10 krad, which allows the installation of the ELMB2 in this area. Figure 3 gives an overview on the full readout chain.

The relatively low update frequency of the ELMB2 (in the order of 6 sec) is not an issue as the data is mainly used for debugging of the performance of the cooling system.
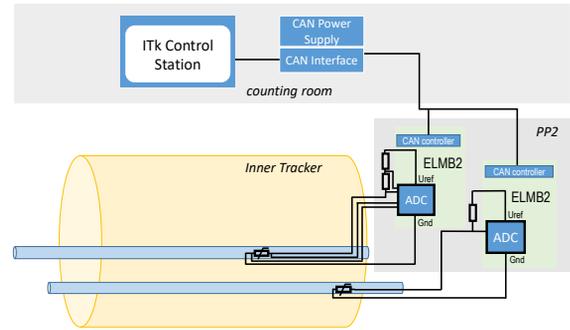

Figure 3: Temperature monitoring.

Humidity Monitoring

The reason for humidity monitoring, respectively the dew point measurement is to prevent condensation of moisture where this can cause harm. The requirements for humidity monitoring inside the strip and pixel volumes are:

- max. dew point -60 °C
- accuracy of dew point: 1 K
- temperature range -55 to +60 °C
- humidity range 0 - 50%
- atmosphere: nitrogen
- operation in magnetic field of 2 T
- radiation level: 900 Mrad
- update rate < 1 min

It is foreseen to use Fibre Optics Sensors (FOS) as they are radiation hard [6].

FOS are fibres with a specific functional coating, which is sensitive to humidity and/or other environmental parameters. The coating of a humidity sensitive fibre absorbs or desorbs water molecules proportional to the humidity, changing the properties of the fibre. Light which is sent through the fibre, either in transmission or in a reflective mode, experiences a change of its spectrum. The change in the light signal is a measure of the absorbed water, respectively the humidity.

For humidity sensing it is foreseen to use LPG (Long Period Grating) sensors, which are "written" onto single mode fibres and are operated in transmission mode. Figure 4 explains the principle of operation. Typically the fibre core is about 10 μm diameter and the co-axial cladding layer is about 125 μm diameter. Ceramic tubes with holes or air gaps will protect the hygrometer.
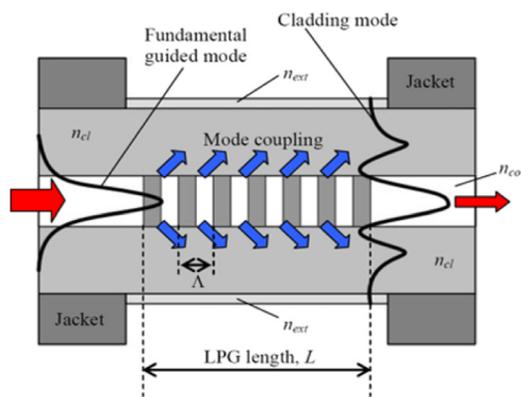
Figure 4: Long Period Grating principle of operation [6].

To decouple the effects of temperature and humidity on the readings of the LPG, a separate thermometry is necessary. A FBG-based (Fibre Bragg Grating) sensor will be used as a thermometer. In the case of the FBG technology a shift of a reflection peak provides the relevant signal information. Pairs of LPG and FBG fibres are foreseen for installation.

Figure 5 gives an overview of the whole readout chain. Besides the sensors themselves all equipment is located in the USA15 counting room. The optical fibres route the signals to the readout system. Central component of the DAQ system is an interrogator, which transmits, receives and analyses the light signals. A PC examines the data further and finally calculates the relative humidity and temperature. An optical switch helps to reduce the number of required interrogator channels. In parallel to the FOS system a sniffer system is foreseen which allows for cross checking and calibration of the FOS system.
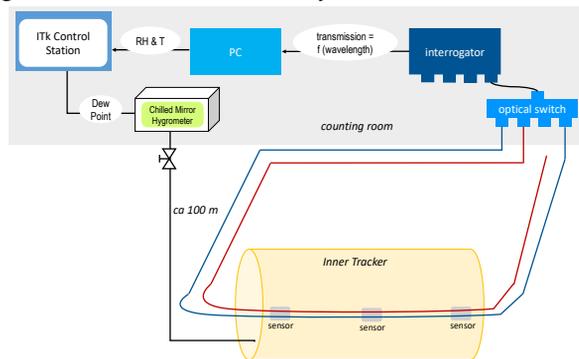

Figure 5: Humidity monitoring.

Radiation Monitoring

The goal of radiation monitoring is the measurement of total ionising dose (TID) and displacement damage in silicon caused by non-ionizing energy loss (NIEL) of high energy hadrons in units of equivalent fluence of 1 MeV neutrons at several locations in the ITk. Radiation doses will be measured with sensors which can be read out online (i.e remotely). This is necessary because of limited access to ITk volume which doesn't allow exchanges of passive dosimeters. TID will be measured by dedicated p-type MOSFET transistors, RadFETs, and 1 MeV equivalent

neutron fluences will be estimated using diodes. The aim of these measurements is to determine the proportionality of doses and fluences with integrated luminosity and compare with simulations of radiation background.

The basic unit is the Radiation Monitor Sensor Board (RMSB) which hosts the radiation sensors.

The online measurement of the Total Ionizing Dose is provided with radiation sensitive MOS transistors (RAD-FETs) in which the dose is measured from the increase of the gate voltage at a given drain current. The readout current pulse is of the order of 100 μA and ca. 1 s long. Displacement damage in silicon is monitored with diodes by measuring the forward diode voltage at a given current. Commercial pin diodes (BPW34F) are used for this measurement. The amplitude of a typical readout current pulse is about 1 mA, and 0.5 s long.

The readout values depend on the temperature, therefore a temperature sensor for monitoring should be added. To provide a stable temperature (as used during calibration) and a controlled annealing of the sensors, the sensors are mounted on a ceramic board and the temperature will be controlled by a current through the resistive layer on one side of the ceramic. Figure 6 shows an example of the complete RMSB package as it was installed inside the current ATLAS Inner Detector [7].
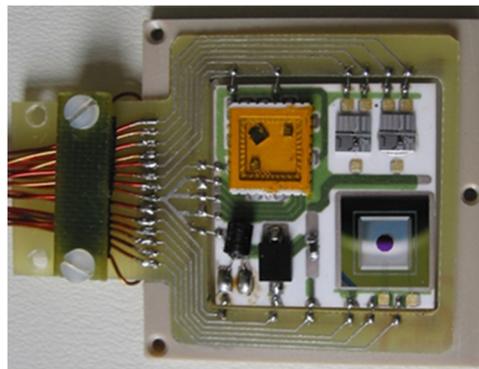

Figure 6: Photo of a RMSB installed in ATLAS ID [7].

In total 28 RMSBs are foreseen, which are distributed in the strip and outer service volume. To ensure sufficient redundancy and to improve measurement accuracy three sensors of each type (3 RadFETs and 3 diodes) will be mounted on each RMSB. We aim for an accuracy of 20%.

The readout system will be based on ELMB2 which will ensure communication with the DCS. ADCs of ELMB2 will be used for measurements of the voltage drop on the radiation sensor. Current pulses of up to 1 mA at up to 100 V bias will be provided by custom made current sources using DACs with SPI communication and will be controlled by the ELMB2. The temperature control unit will also be steered via the ELMB2. As long cables have no severe impact on these measurements, the ELMB2 and the related current sources can be installed in the counting room.

THE ITk INTERLOCK SYSTEM

The ITk common Interlock system is a safety system. It is a hardwired system as last line of defense. An autonomous operation is necessary and the system must be operating all the year. Major risk for all silicon detectors are heat-ups. Mainly power supplies are controlled by the interlock system. Independent monitoring of the signals is added for debugging.

Concept of the Interlock System

Figure 7 explains the concept of the interlock system. Sensitive detector elements are protected by temperature sensors. The analogue temperature value is by means of a discriminator translated into a binary signal (ok, error) and routed to an Field Programmable Gate Array (FPGA), which houses an interlock matrix and is the core of the interlock crate. The interlock matrix defines the actions which should be executed in case of an error, e.g. if a detector unit becomes too hot, the related power supplies will be switched off. Signals from external systems can be integrated, e.g. signals from the cooling plant or from the ATLAS wide safe-for-beam interface. Vice versa signals to external systems can be generated. This might become necessary during the bake out of the beam pipe.
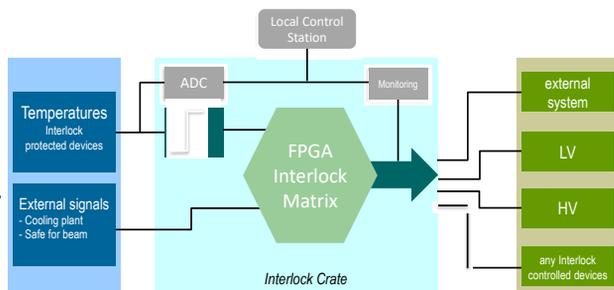

Figure 7: Concept of the interlock system.

For debugging a monitoring system is integrated into the interlock crates. It allows for monitoring the analogue values from the temperature sensors and also spies on the signals, which are transmitted to the power supplies. But there is no possibility to overwrite the interlock signals via the DCS software. Core of the monitoring system is another FPGA (Mon-FPGA) which collects data and provides the interface to the local control station. As the interlock system is a safety system its operation is completely independent from the availability of the monitoring system.

Requirements of the Interlock System

The design of the interlock hardware is driven by the needs of the sub-detectors. An inventory of temperature sensors and power supply (PS) channels added up to the number of channels, which should be handled by the interlock system, see Table 1.

There still might be some small variations in the final numbers, anyhow Table 1 shows that a huge number of channels must be handled by the interlock system. The

Table 1: Number of Interlock Channels

	temperature sensors	PS
pixel	1012	4220
strip	1552	5200
total	2564	9420

main reason for that large number is, that the power supplies are controlled with a high granularity in order to keep the number of detector elements, which are out of operation, always at a minimum. The large number of channels also explains why no commercial solution was selected.

The interlock system must also provide a lot of flexibility. As already can be seen from Table 1 the needs of strip and pixels differ, but also the needs of the sub-detector vary for different parts of it. Additionally, it might become necessary that the logic must be changed due to changes in the detector hardware (e.g. signal of a temperature sensor is lost) or the user decides for another interlock strategy.

Besides the protection against local heat-ups of detector elements, the interlock system should protect against the following risks:

- Failure in the cooling plant
- Failure in the gas flow
- Unsafe beam conditions
- Bake out of the beam pipe
- Smoke in the detector

Provided hardware signals are available, the interlock system could also protect against other risks, e.g. caused by the use of lasers.

Realization

For the temperature sensors which are located on the strip and pixel detector elements 10 kΩ Negative Temperature coefficient (NTC) sensors were chosen. Their large temperature coefficients allow to use long cables (ca. 100 m) between the NTC and all interlock circuits. Thus all interlock electronics can be located inside the radiation safe counting rooms.

The interlock system will consist of 19" interlock crates, which are built in a modular way. This approach was already used for the construction of the interlock matrix crate of the ATLAS Insertable B-Layer [8] and provides sufficient flexibility. One interlock crate should be able to handle up to 576 IO signals.

According to the needs of the sub-detector the crate can be equipped with different type of modules. It will be a 3U high 19" crate. Besides the slots, which are occupied by the Interlock-FPGA and the Mon-FPGA, it has 18 slots, where modules with different functionality can be installed.

Actually three different type of modules are under construction:

- T2I module
- OUT module
- GSS module

The back panel routes the signals between the modules and the FPGA boards. Due to the large number of channels

to be handled by one interlock crate, IO-expanders are used to transfer the signals between the modules and the FPGAs. A further advantage of the IO-expanders is that they allow for the selection of FPGAs with a limited number of IOs.

The Temperature 2 Interlock (T2I) module handles the analogue signals from the temperature sensors. By means of a discriminator circuit it transfers the analogue signal into a binary information. The OUT module is the standard module, which routes the signals from the FPGA onto the different LV and HV power supplies. The signal levels are adapted to the needs of the interlock inputs of the power supplies. The General Safety Signals (GSS) module is an IO module for interconnection to external systems. It can receive signals from external and translates them into signals, which can be fed into the Interlock-FPGA, (eg. by reading the status of current loops) vice versa it can modify signals from the FPGA to the required signal, which is adapted to the inputs of an external system (e.g. level shifters).

Core of the interlock crates is the Interlock-FPGA module, based on an Artix7 FPGA from Xilinx (XC7A200T-2C). Its firmware takes care of the proper handling of the hardware and is the same for all interlock crates. Just the configuration of the FPGA registers and the logic program differ between interlock crates and are adapted to the logic which the user wants to apply.

Main component of the monitoring module is a FPGA from Intel (MAX 10M family). The monitor module is intended to provide debugging information when abnormal situations are detected by the interlock module and to provide data logging functionality for problem analysis. It can also generate test signals. These are not used during normal operation. They are restricted to debugging or testing during dedicated time periods. These test signals can create artificial interlock signals, but they can't overwrite existing ones. Due to the required flexibility of the interlock crate the monitoring module must be able to handle:

- 288 ADC channels
- 576 digital inputs and
- 288 digital outputs

The Mon-FPGA reads the analogue values from the temperature sensors, the output values from the temperature discriminators and also spies on the interlock signals which are transmitted to the power supplies.

The information is transmitted to the address space of an OPC-UA server, which is the interface to the standard ATLAS control system.

ITEGRATION INTO ATLAS DCS

The ATLAS wide DCS is built in a tree structure composed of more than hundred Local Control Stations. There is the Global Control Station (GCS) at the top [9], the sub-detector control and the local control stations forming the underlying layers. The GCS provides the main user interface for operation of ATLAS.

To have an homogenous interface for all sub-detectors, for the implementation of ATLAS DCS a commercial Supervisory Controls and Data Acquisition (SCADA) system

was chosen: WinCC by Siemens (former PVSS by ETM). With its inter process communication and distribution managers it allows for connecting a large number of control systems to one entity.

A finite state machine models the hierarchical structure of ATLAS DCS. Its top level, representing the ATLAS detector, is running on the GCS, with the sub-detectors and their equipment being the children. They receive commands from the top and propagate status information from bottom to the higher levels.

As software protocol for communication Open Platform Communications Unified Architecture (OPC-UA) is foreseen and should be used where ever possible. Once the sub-detector data is available in the data space of an OPC-UA server, one profits from all the tools which are provided by central ATLAS DCS. This includes user interfaces for operation, data archiving, generation of Alerts and the interfaces to external systems.

As the design of the temperature and radiation monitoring systems are based on the ELMB2, the integration of their data is covered by an existing OPC-UA server. The integration of the humidity monitoring and the monitoring data of the interlock system will require some efforts by ITk. It is planned to make use of quasar [10], which provides a frame for users to build their own OPC-UA servers.

SUMMARY

A large silicon based tracker is under construction for the ATLAS experiment at the HL-LHC. For safe operation a very reliable detector control system is required. While the monitoring and control of all detector elements is provided via the interfaces of the detector power supplies or sub-detector specific ASICs, the ITk common system monitors the environmental parameters. Most demanding are the required accuracy, the radiation hardness and the inaccessibility of the sensors for years. While the temperature and radiation monitoring systems are based on Pt sensors, RadFETs and PIN diodes, the humidity monitoring will make use of LPG Fibre Sensors, a relatively new technology. In case of risky situations an Interlock system, which is a hardwired protection system, ensures the safety of the detector.

The readout of the sensors and the monitoring of the interlock system require different data acquisition systems. These are chosen and first prototypes are currently built. Where available standard ATLAS components will be used, while sensors like FOS require commercial solutions. OPC-UA servers will be used as communication software for integration into WinCC, which is the ATLAS standard control system.

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