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CENBG CONTROL SYSTEM AND SPECIFIC INSTRUMENTATION DEVELOPMENTS FOR SPIRAL2-DESIR SETUPS

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Abstract

The DESIR facility will be in few years the SPIRAL2 experimental hall at GANIL dedicated to the study of nuclear structure, astrophysics and weak interaction at low energy. Exotic ions produced by the S3 facility and SPIRAL1 complex will be transferred to high precision experiments in the DESIR building. To guaranty high purity beams to perform high precision measurements on specific nuclei, three main devices are currently being developed at CENBG: a High Resolution Separator (HRS), a General Purpose Ion Buncher (GPIB) and a double Penning Trap named “PIPERADE”. The Control System (CS) developments we made at CENBG are already used to commission these devices. We present here beamline equipment CS solutions and the global architecture of this SPIRAL2 EPICS based CS. To answer specific needs, instrumental solutions have been developed like PPG used to optimize bunch timing and also used as traps conductor. Recent development using the cost efficient Redpitaya board with an embedded EPICS server will be described. This device is used to drive an FCup amplifier and is also used for particle counting and time of flight measurements using our FPGA implementation called “RedPiTOF”.

THE DESIR FACILITY

Overview

In 2024 DESIR [1, 2] is planned to be the new low energy SPIRAL2 facility dedicated to the study of nuclear structure, astrophysics and weak interaction at GANIL (Caen, France). This experimental building will accept low energy (10-60 keV) RIB beams from both historical SPIRAL1 complex [3], delivering heavy ions beams since 1983 and the new SPIRAL2 linear accelerator [4] via the S3 facility [5] delivering high intensity light ion beams since 2019 (see Fig. 1). In DESIR, specific exotic ions will be separated in mass and transferred to high precision experiments to perform decay spectroscopy, laser spectroscopy and mass spectrometry.

CENBG Developments

In order to provide highly purified beams previously introduced, three main devices have been entirely developed and are currently tested and commissioned at CENBG: a High Resolution Separator (HRS) [6], a RFQ-cooler-buncher called “General Purpose Ion Buncher” (GPIB) [7] and a double Penning Trap named “PIPERADE” [8].

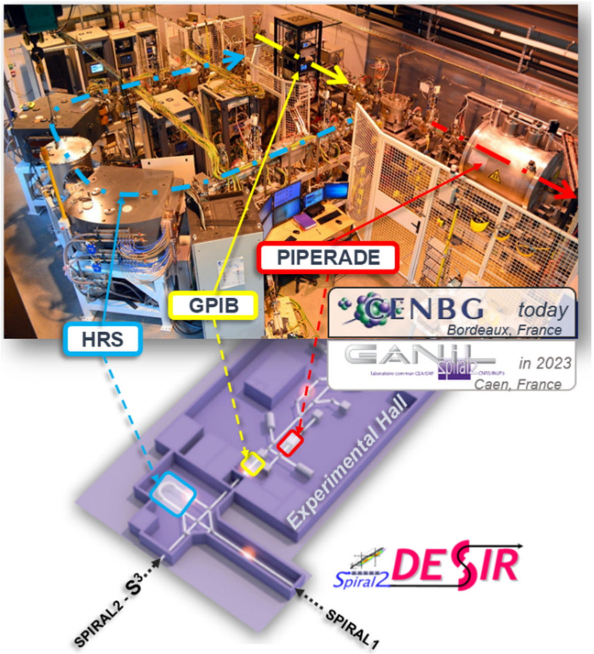

Figure 1: The CENBG setups today at CENBG and the future DE-SIR experimental area, coupling the GANIL building and the new SPIRAL2 facility.

The main concepts of the control system (CS) developed and currently used to test and commission the HRS, the GPIB and PIPERADE is presented in this paper. These CS developments done at CENBG will be extended to the entire DESIR project, meaning to the four DESIR transfer lines (180 meter long):

1. LS: beam transfer from S3 to the DESIR Hall.
2. LT: beam transfer from SPIRAL1 to the DESIR Hall.
3. LHR (High Resolution beamline) including a dedicated RFQ-Cooler SHIRAC (LPC-Caen) and the HRS.
4. LHD (DESIR Hall Beamline): Central delivery “fishbone” line inside the DESIR Hall.

Milestones

The DESIR beam-lines and the experimental Hall equipped with the first group of experiments are expected in 2023. The HRS separator and PIPERADE traps are already in the commissioning phase at CENBG using the first version of the DESIR control system.

DESIR CONTROL SYSTEM (CS)

SPIRAL2 Collaborative Developments

The DESIR CS and Automation developments for the whole beam-lines and purification devices including the

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PIPERADE apparatus are done at CENBG. In order to ensure the compatibility with the already existing SPIRAL2 LINAC accelerator and NFS, S3 experimental areas, these developments are carried out in close collaboration with the GANIL laboratory. It is based on the Experimental Physics and Industrial Control System (EPICS) architecture [9], basic framework for the SPIRAL2 control system [10, 11]. Among the accepted common rules is the naming convention used at SPIRAL2 applying to equipment names as well as CS Server names including EPICS process variables.

EPICS servers (IOC) are developed within the “topSP2” common software platform based on the CentOS Linux system running on PC configured like SP2 CS computers. All of them run the same EPICS base 3.14.9 and share versatile IOCs/EPICS modules dedicated to various equipment like GANIL beam profilers (harp wire monitors) or Hazemeyer power supplies for the HRS electromagnetic dipoles.

Up to now our CS software developments are directly saved and versioned on the GANIL SVN server and a migration to the Gitlab server of the CNRS/IN2P3 institute is planned next year. Software development tools are shared with the GANIL CS group like the Spiral2 version of CSS/BOY (CSS-Dev & CSS-Op) developed under ECLIPSE IDE [11] and used to build most of GUIs. Phoebus [12], the current variant of CSS not depending on Eclipse RCP, is planned to be used in the future to develop DESIR beamlines HMI. Some “Rich” Clients like the “ProfilSP2” Java Application developed at GANIL also operates at Bordeaux during the commissioning phase. Finally, the DESIR beam-lines IOCs for PLC driven equipment communicating with servers using Modbus-TCP protocol will be generated by the GenIOC utility [11].

CS Architecture and Main Options Followed

The DESIR CS architecture is based on EPICS Client-Server system deployed on an Ethernet network using the Channel Access protocol. The management of the vacuum and interlock systems is made via automation as detailed in the following paragraph. This architecture is illustrated in Fig. 2 with the PIPERADE CS example.

For PIPERADE, some equipment are localized on a high voltage platform (~ 30 kV) because the Penning trap itself had to be at this potential to decelerate ions coming in. In this case, unmanaged Ethernet Moxa switches are used with fibber optic port to guaranty the galvanic insulation of equipment without reducing communication.

Most of the EPICS servers are executed as services on a Linux (CentOS) Machine. For DESIR, embedded IOCs have been considered for High Voltage Power Supplies (HV-PS) and Redpitaya boards described later in this paper.

VME crates with embedded EPICS servers are still used in SPIRAL2 for historical reasons to answer high speed data acquisition needs, but also low speed digitizing, digital I/O and analogue signal generation. In 2018, the DESIR project decided not to use VME at DESIR.

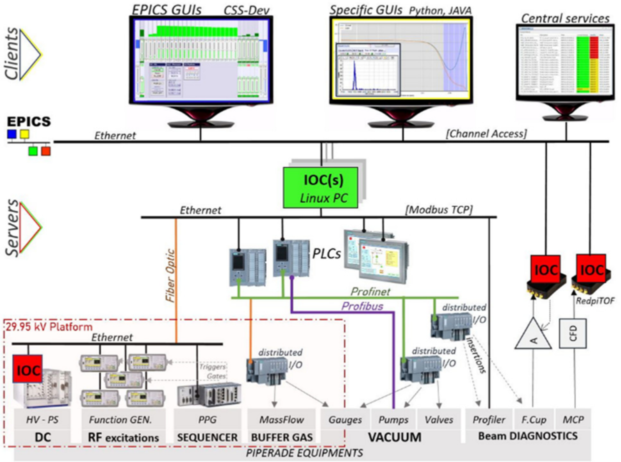

Figure 2: Overview of the PIPERADE CS architecture. Equipment are illustrated on the lower part of this figure. These hardware are controlled by PLCs (Automation part) or directly by EPICS servers (IOC). Ethernet network is the main communication media and Fieldbuses like Profibus and Profinet (Profibus on Ethernet network) are used by PLCs. On the upper part of this figure, Clients are the applications used to control the PIPERADE experiment.

An innovative solution, as detailed in the following automation section of this paper, has been experimented and validated at CENBG to replace VME boards regarding the low speed Faraday Cup (FCup) control and signal digitizing.

Automation Overview

All SPIRAL2 vacuum systems and interlocks are managed using dedicated PLCs (Siemens S7-1500 series) [13]. They are similar to the systems developed by the GANIL CS & Automation group except some improvements hereafter exposed.

As figured in Figure 2, each beamline will have its own Vacuum PLC and Interlock PLC coupled with their own touch panel (local HMI). DESIR PLCs will be localized in a control room far from equipment and will communicate via the Profinet network with distributed Input/Output (I/O) modules (ET200S) deployed in the racks along beamlines. When ET200S are needed on high voltage platforms like the GPIB or PIPERADE, “classical” Ethernet fibber optics are used.

According to the SPIRAL2-Phase1 standard (LINAC, NFS and S3), a “vacuum” PLC unit manages all pumping groups (Pumps, Gauges and Valves) and gas systems (like mass-flow controllers) for a beamline sector. In parallel, Profibus fieldbus allow to collect “live” information from turbo-molecular pumps like the rotation speed or detailed status or fault words.

In addition to the vacuum PLC, a dedicated “interlock” PLC is also affected to each beamline. It interlocks the equipment according to the safety conditions like veto on the high voltage power supplies but also controls all beamline insertion devices like electro-pneumatic translators to put diagnostics IN or OUT the beam axis.

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Modbus-TCP servers are implemented in PLCs to manage the communication with dedicated IOCs. The vacuum Modbus table is made of read-only Registers. On EPICS side, only the valves status and pressure values are exchanged and displayed on operator interfaces. Actions on vacuum devices are only authorized using PLCs touch panels, even in remote mode with VNC Clients. WinCC client software will be used at GANIL to develop centralized vacuum interfaces.

New PLC Based Controlled Beamline Equipment

DESIR Interlock PLCs are driving two other kind of equipment: Faraday cups (FCup) and motors.

DESIR beamline FCups are used with “PicoLIN” transimpedance amplifiers [14] developed at GANIL for CW low intensity beam measurement: 8 ranges from 10µA/V down to 1pA/V are selectable. This amplifier is directly controlled in remote mode with the Interlock PLC ET200S Digital I/O and the output signal is sampled and digitized with a 16bit ADC from the same ET200S. This solution used for the HRS tests and commissioning since 2017 is adopted for all DESIR FCups.

The other “new” equipment controlled by PLCs are motors used for the HRS Slits positioning (20 motors), and will be used for six electrostatic 90° beamline deflectors to place or remove them from beam axis. Brushless motors have been selected (Siemens ref 1FK7015) and equipped with a brake to maintain the position when the motor power is switched off (after 1 minute timeout). Classical position encoders with optical disk are not radiation hardened. This is the reason why we preferred these motors with multipole resolvers. Each motor is driven with a Siemens CU-310 one axis control unit and a Siemens PM340 power module. The communication with the Interlock PLC is based on Profinet fieldbus.

SPECIFIC SOLUTIONS FOR DESIR EQUIPMENT

“Heavy” Client’s Developments

The EPICS CA protocol makes it possible to monitor and control any beam line equipment through PV calls in many programming languages.

Using EPICS features, a Python program is under development to operate the PIPERADE traps, i.e. scan the different trapping and excitation parameters, define the time sequence and treat on-line measurements. It is inspired by the PyMassScanner program developed by the JYFLTRAP group (Jyväskylä University, Finland) [15] part of our collaboration.

Other Python software tools have been developed at CENBG to answer tests and commissioning needs for the GPIB and PIPERADE. The first example is “Plotpot” which displays the electric field seen by ions in Paul or Penning traps with respect to voltages applied on *the* electrodes. A second example is the automatic beam injection with a multiparameter algorithm based on a simplex optimization method.

“CorrAb” is another tuning application under development at CENBG for the HRS optimization. It will be used to estimate the separator aberrations using a dedicated emittancemeter and then apply the computed voltages to the 48 poles of the HRS multipole to correct as much as possible the separator aberrations. The goal is to reach a resolution of 20000 for isobaric separation using this software.

High Voltage Power Supplies (HV-PS)

Most of the DESIR beam-lines and setups are composed of electrostatic optics: Quadrupoles, Hexapoles, Benders and Steerers.

In order to meet the High Voltage-Power Supplies (HV-PS) requirements (optics and diagnostics), ISEG multichannel crates provide all DC voltages (see Fig. 3).

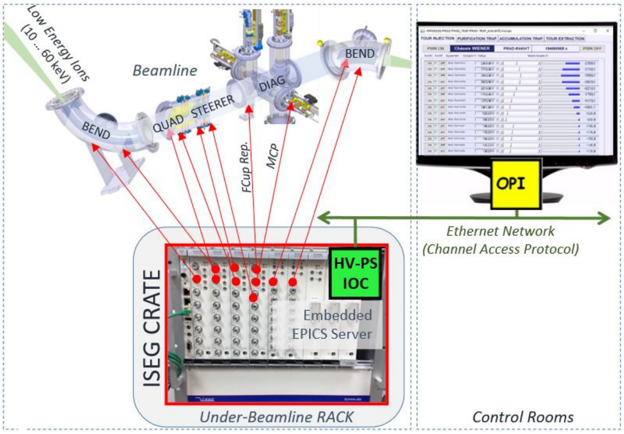

Figure 3: Hundreds of high voltage power supplies (HV-PS) will be deployed under DESIR beamlines and setups. Each multichannel ISEG crates will concentrate a large number of HV-PS and its CC24 controller will run the embedded EPICS server making this solution very “light” and easy to maintain. CSS Operator interfaces are already used to control sets of HV-PS to tune DC electrical fields.

Since 2017, more than 200 HV-PS channels are used at CENBG for the HRS, GPIB and PIPERADE.

Pulse Pattern Generator (PPG)

Ion traps such as PIPERADE need a configurable real-time “conductor”. This sequencer also called PPG has been developed for GSI-SHIPTRAP and CERN-ISOLTRAP [16] on RIO FPGA, Real-Time PCI boards with LabVIEW software. We developed seven years ago a PPG for PIPERADE reusing the same LabVIEW FPGA State-Machine on a CompactRIO (NI-7410) to generate time sequences over 32 digital outputs with 10 ns time resolution. High speed LVTTL modules (NI-9402) trigger Agilent function generators (Traps RF excitations) and gate home-made high-speed and high voltage switches (ions injection – transfer - extraction).

The PPG IOC is running on the remote Linux PC to benefit from a “real” EPICS server with full functionalities compared to the uncomplete LabVIEW EPICS Server.

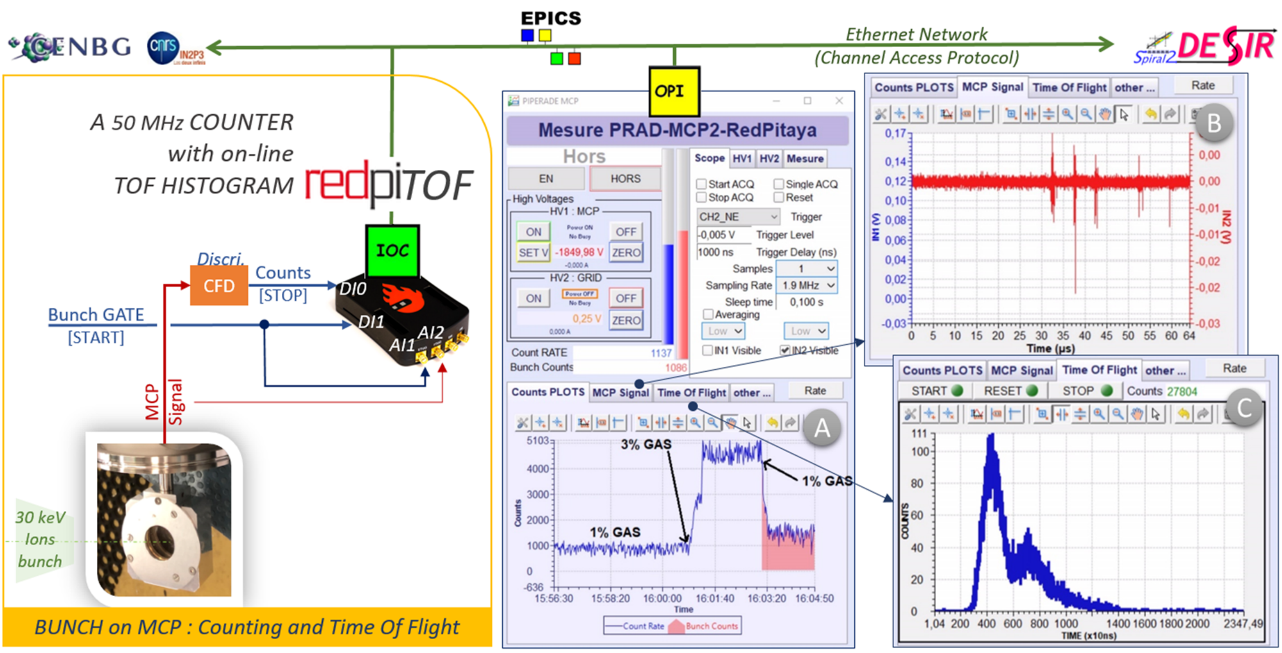

Figure 4: Illustration of our RedpiTOF device developed on a Redpitaya board to count ions detected by a micro-channel-plate (MCP) and measure the Time Of Flight (TOF) with 10 ns time resolution. The TOF histogram (C tab) is constructed on-board and the embedded EPICS IOC allows EPICS Clients to control it. Counting rates (see “A” tab on figure), MCP analogue signal (see “B” tab) and TOF histogram (see “C” tab) are monitored online on the RedpiTOF CSS Operator Interface.

A LabVIEW EPICS Client is running in the CRIo and “feed” the IOC to control the PPG (time sequence definition and start/stop controls) and update the current PPG status with configuration read-back values.

The same PPG device has been cloned to control via five HV fast switches the GPIB buncher time sequence and define the bunch time structure.

Redpitaya for Beam Diagnostics

Bunch intensity on FCup Bunched ion beams produced by the GPIB RFQ-Cooler-Buncher have to be characterised. Hardware solutions are needed to measure the time dispersion, longitudinal emittance and energy dispersion of these microseconds length bunches produced with a slow repetition rate (few bunches per second).

In mid-2019 we chose the cost efficient Redpitaya (RP) board (STEMLab 125-14) to monitor high intensity ion bunches. This choice was motivated by:

- The High performance “dual channel scope” (125 MSamples/s; 14 bits ADC on +/− 1V input signal).
- The board size and SMA connectivity: Easy integration close to beam diagnostics without any hardware development.
- Its Digital Inputs/Outputs usable to drive an amplifier and check its status
- Its Linux operating system (Ubuntu) with the embedded EPICS IOC already developed by the Australian Synchrotron [17].
- The relative low-cost of this complete solution.

A high-speed transimpedance Femto amplifier (DHPCA) amplifies and converts the collected charges of a FCup into a voltage signal. This amplified signal is then injected in one of the two RP SMA analogue input and an operator interface is able to monitor the acquired high-speed signal from the waveform process variable generated in the embedded IOC. The amplifier range is remotely selected using some digital I/O also used to read the amplifier status.

Counting and timing with RedpiTOF Ion counting and TOF measurements using a Micro Channel Plate (MCP) detector are required for PIPERADE trap measurements and GPIB commissioning. Although counting and coincidence solutions have already been developed on RP boards [18, 19], we started the RedpiTOF development in end-2019 (see Fig. 4).

In addition to the RP scope and wave generator IP, new counting and TOF functionalities using two 100 MHz digital inputs (DI) have been implemented on the Xilinx FPGA and dual core ARM (see Fig. 5). This new “device” is based on a 50 MHz counters (100 MHz clock) and a real-time TDC with 10 ns time resolution implementation.

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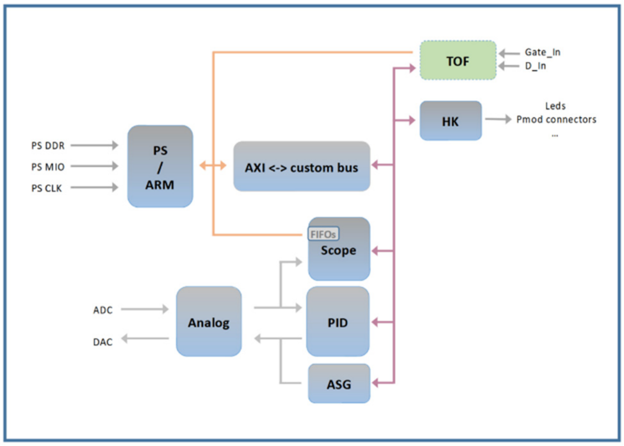

Figure 5: Overview of the firmware architecture. It illustrates how the new TOF function (in green) is interfaced with the original system (in blue).

The first DI is used as a “Gate” signal. The TDC “starts” on a rising edge, while the second DI is “reading” ion signals and act as the TDC “Stop” on rising-edge signal coming from the detector (MCP) discriminated output.

This development has been completed last year with the on-board 16k channels TOF histogram construction, controls (start, stop and reset) and bin size selection (10 ns to 80 ns) to permit TOF dynamic up to 1.3 ms (see Fig. 6).

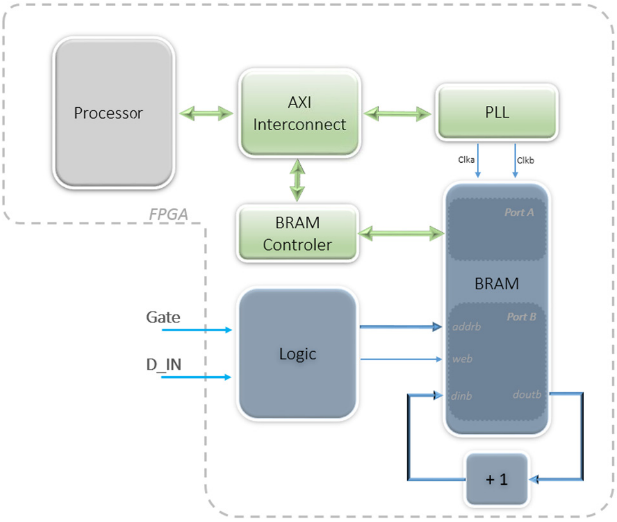

Figure 6: Here is the architecture of the RedpiTOF FPGA implementation. Histogram construction is based on the use of a dual Port RAM. The two digital inputs are processed into the logical module (Logic) to address the first RAM port and increment the value of the selected memory register (Memory address = TOF channel number). The second port is used by the processor to read the histogram over AXI bus with the EPICS driver.

Since January 2021, two RedpiTOF boards are daily used: one for the GPIB bunch characterisation and the other for PIPERADE pennings traps.

CONCLUSION

The Control System (CS) developments we made at CENBG are already used to test and commission the HRS separator, the GPIB RFQ-Cooler-Buncher and PIPERADE penning traps. These slow control CS developments have to be extended to the LS, LT, LHR and LHD DESIR beamlines composed with the same electrostatic devices and diagnostics.

Some CS solutions have to be improved in the following years, in particular for beam diagnostics like low intensity current measurement systems needed for bunched beams and an emittancemeter.

We are also preparing the migration on Phoebus to develop most of the operator interfaces and we will use our institute Gitlab IN2P3 for all of our software developments, up to now using a Subversion repository.

The collaborative work with the GANIL CS team is continuing to prepare as much as possible the DESIR beamlines commissioning at GANIL programmed in 2024.

ACKNOWLEDGEMENTS

This work has also been performed with the helpful contribution of PIPERADE and HRS teams, thanks for their feedback and advice as users of these developments.

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