# THE HV DCS SYSTEM FOR THE NEW SMALL WHEEL UPGRADE OF THE ATLAS EXPERIMENT

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### Abstract

The background radiation at the HL-LHC is expected to exceed the one designed for the ATLAS muon spectrometer. In order to cope with the foreseen limitations, the collaboration decided to replace the Small Wheel (SW) with a New SW (NSW) by combining two prototype detectors, the small-strip Thin Gap Chambers or sTGC (STG) & and resistive Micromegas (MMG). Both detector technologies are "aligned" to the ATLAS general baselines for the NSW upgrade project [1], maintaining in such way the excellent performance of the system beyond Run-3. Complementary to the R&D of these detectors, an intuitive control system was of vital importance. The Detector Control System (DCS) for both the MMG and the STG High Voltage (HV), have been developed, following the existing look, feel and command architecture of the other sub-systems. The principal task of the DCS is to enable the coherent and safe operation of the detector by continuously monitoring its operational parameters and its overall state. Both technologies will be installed in ATLAS and will be readout and monitored through the common infrastructure. Aim of this work is the description of the development and implementation of a DCS for the HV system of both technologies.

### OVERALL VIEW OF THE NSW HV DCS SYSTEM

Figure 1 illustrates a simplified sketch of the New Small Wheel. The wheel consists of 16 sectors equally divided into large and small sectors. However, the detector geometry is different for each sector type. The numbering of the sectors begins at the left large sector with number 1 and continues clockwise, similarly to the realization in DCS. All large sectors have odd numbers (1,3,5,7,9,11,13,15) while the small ones have even numbers (2,4,6,8,10,12,14,16). Each sector is equipped with the so-called quadruplets of both detector technologies. One quadruplet consists of four layers of a certain detector type.

### MMG Scheme

The Micromegas sectors are divided into two quadruplets in radial direction. The quadruplets close to the beam axis defined as xM1, and the outer ones with xM2. Small and large quadruplets just differ in dimension, while similar size layers (xM1, xM2) differs in the number of Printed Circuit Boards (PCB). The larger ones consist of five single readout PCB's which are mounted together to form a detector layer



Figure 1: Representation of the NSW (top) with the relevant positions of the NSW sectors, (sTGC and MMG, Small & Large). The different sTGC and MMG modules composing a small sector of the NSW (bottom).

of a quadruplet. On top of the PCB the readout lines are located.

**HV Modules Requirements:** For both MM quadruplet types a nominal voltage of  $570 \text{ V}/128 \mu\text{m}$  for the readout is foreseen. The drift boards are supplied by a voltage of 300 V. The current is expected to be less than  $1 \mu\text{A}$  for a readout HV channel. One channel serves one PCB, while the number of channels of all modules sum up to 1024.

### sTGC Sheme

The sTGC detectors are divided into 3 quadruplets in the radial direction. The quadruplets naming in radial direction uses the partition definition of inner, middle and outer. A special characteristic is that the innermost quadruplet of the sTGC is divided into two HV sectors in radial direction, due to higher particle flux close at the beam pipe.

**HV Modules Requirements:** The sTGC quadruplets are operated only with one voltage of around 2.8 kV. There is no aggregation of channels planned, as the number of channels of all modules sum up to 1024. The chosen limits are 1 mA for the innermost HV sector of the inner quadruplets and 0.5 mA for the remaining ones.

### Overview of the DCS Internal Structure

In order to incorporate the hardware information into the DCS, several components have been used or developed within the scope of the JCOP Framenwork [2]. Datapoint Types (DPT) have defined for each hardware component, device and detector segment. Their instances, namely the

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datapoints (DP), contain all the information (DP Elements) needed in order to describe all the parameters (configs). Additionally, a DP generator developed and programmed to map and set up all the necessary DPs to their associated HV channels., which will be used as the base of the system. In order to translate this structure, to something more meaningful and user friendly, a set of panels has been developed, for the control, monitoring and configuration of the HV system. Finally, a control manager is under development, in order to adjust the high voltage as a function of the pressure and the temperature.

### ARCHITECTURE AND HARDWARE REQUIREMENTS

The detailed architecture of the local DCS relies on the structure of the general DCS system of the ATLAS experiment and on the electronics architecture. Each sub-detector is implemented and organized in a unique way but it must also conform to the guidelines defined by the ATLAS central DCS [3,4]. When special requirements need to be handled by the detector then tailored solutions must be applied.

#### Architecture

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Content

The system architecture consists of several components based on the sub-detector needs and it is supplied by the Universal multichannel CAEN system. The hardware architectures of each sub-system are depicted in Figs. 2 and 3. The MMG chain, the simplest one, consists of 3 SY4527 mainframes [5] that host, supply and control 2 different type of HV boards, A7038ST(P/N, x10 in total) & A7038AP (x16).



Figure 2: The hardware chain of the MMG as has been installed at ATLAS P1.

The STG chain consists of 2 A1676 branch controllers [6] installed on a SY4527 mainframe, controlling 4 Easy3000s crates [7], hosting 6 HV boards (x3 A3535AP & x3 A3540AP).

Both the easycrates and the easyboards are supplied by two external DC power of 48V generated by separate AC/DC converters. The first generator of type A3485, provides the Service power, needed to control the devices, while the second one of type A3486, is used to supply the line with power. Each generator is controlled by a dedicated branch controller.

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Figure 3: The hardware chain of the STG as has been installed at ATLAS P1.

The communication between the hardware and the DCS is achieved via the OPC UA server-client pairing [8]. Both are deployed on the host servers with the OPC UA clients gathering the address space of the individual channel parameters, transmitting them to the main control stations. The graphical user interface (GUI) of the generators is depicted in Fig. 4, while for the mainframe's monitor and control a dedicated panel is shown in Fig. 5.



Figure 4: Service projects for the monitoring of the 48V ACDC Generators.



Figure 5: Service projects for the monitoring of the SY4527 mainframes.

### Requirements

The DCS is responsible for the safe and coherent operation of the detector. All ATLAS sub-detectors have their own local DCS, controlling and monitoring the sub-detector and its equipment. Among its core requirements are:

- Remote control, monitoring and configuration of a wide variety of parameters, like voltage and current set/read-back, state and status values along with error flags.
- Active archiving with smoothing and on-the-flight storage in the DCS database [9].
- Data exchange with other sub-systems.
- Discrimination between radiation sensitive and hard parts,
- Compatibility with operation under radiation and magnetic field as in the ATLAS cavern.
- Automated mechanisms, such as the safety Interlock, the Reset Trip, the HV transition when the Beam for Physics is expected or not, etc.
- Communication is established via the OPC UA serverclient pairing.

# FSM HIERARCHY AND LOGIC

As a detector oriented hierarchy the control system is represented by an homonymous Finite State Machine (FSM) [4] node (MMG/STG). The top node defined as the main control unit, and from there commands are propagated downwards into the device or logical elements. Such units, groups and geographical detector segments are represented by deviceoriented (SMI) FSM objects. The current condition of each object is determined by a set of states alongside with their transitions. A state transition is triggered either by a condition change or by a dedicated action. Figure 6 depicts the device and logical state diagrams. It allows a device to change from its ground state OFF to its operational state ON via optional stages, while for logical objects, the mandatory states are READY or NOT READY, reflecting conditions for which data taking is possible or not. The state UNKNOWN is used when the condition cannot be verified for both cases.

Figure 7 shows an instance of the MMG FSM tree along with each commands. The actual state is determined by the states of the associated children via state rules implemented using SML and they propagate upwards. Custom-made actions can be defined easily via the read control scripts, i.e. interlocking or resetting the flag of a channel, complementing the system.

## **OPERATION PANELS**

Both projects have been developed, following the existing look, feel and command architecture of the other Muon subsystems, in order to facilitate the shifter/expert operations.

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Figure 6: Device (left) and Logical (right) object state model.



Figure 7: MMG FSM Tree instance at chamber level.

For each individual layer, a main panel has been developed, providing the user with useful information, reflecting the state and status of the detector. All the vitals of each layer can be displayed in trend-plots or/and tables; while a secondary panel provides supplementary to the main panel details.

A general review of the graphical user interface of the top FSM nodes and their constituents are shown in the Figs. 8–13. To facilitate the experts' work also advanced panels and colormaps of the system have been developed. A typical example of a colormap, used by the MMG, is shown in Fig. 13.

# Side View

The shifter/expert in the Atlas Control Room usually will have an overview of the sub-system. The typical view for the MMG technology is shown in Fig. 8, where 10 wheels are displayed. As the number of HV sectors within the MMG quadruplets is identical to the partitioning of the quadruplets, their representation in the panel can be retained. The sTGC sectors, seen in Fig. 9, have 3 quadruplets, but 4 HV sectors in radial direction. Therefore, 4 indicators are shown for each sector of the sTGC. Each wheel represents the quadruplets, either close to the IP or HO side. The color indication of the trapezoidal and its accompanied circle refer to the FSM State and Status of the complete quadruplet., respectively. Furthermore, both shapes feature different actions depending on left-, right- or double-clicking [10, 11].

# Sector View

The dedicated to the sector panel is shown in Fig. 10. On the top the chosen sector is indicated in a text field. A table is displayed, where all the key parameters for each layer of the quadruplets of the chosen sector are shown. These are the name and location of the connected HV board and channel



Figure 8: Operational Panels for the MMG sub-system.



Figure 9: Operational Panels for the STG sub-system.

as well as the actual values of voltage and current, accompanied by their error flags. Below the table the connected HV modules are shown, together with additional information of the type, the connection pattern, the temperature, the serial number and the error flags. Complementary to that, a manipulation section on the configuration has been added for convenience during the commissioning at P1 [10, 11].



Figure 10: Operational Panels for both MMG and STG subsystems.

#### Chamber View

In case that a more detailed view of a quadruplet is desired, the panels in Figs. 11 and 12 can be called. In the top the name of the quadruplet is given. Below the name of the quadruplet the names of the connected HV modules are displayed, including their periphery of mainframes, branch controllers, etc. On the right side of the names there are buttons which allows the user to navigate to the corresponding panel, which holds the information about the selected module. Below the fields for the HV modules a table shows more details about the connected channels, their set and monitored voltage or current. The last column of the table shows the errors and has a color-changing indication for fast reading. On each cell of the table, the right-click functionality is enabled. This triggers the instantiation of a trend plot which pops below the table. The trend plot is automatically updated if a change in the values occur. In contrast to this, the table is only updated if the "refresh" button is used. Furthermore, a so called "expert mode" is implemented, followed by the chamber overview panel. This allows shift experts to modify the values of voltage or current of the displayed channels [10, 11].



Figure 11: Operational Panels for both MMG and STG subsystems.

### Layer View

User can navigate lower to the hierarchy, to the so-called Layer View. Here is the main difference between the p2 rojects. For the MMG project, the layer belong to the family of the LUs while for the STG belong to the DUs. Thus, it will be presented at the next subsection. Figure 12 depicts the layer view of the MMG. There the overview picture can be taken for the all the layer's PCBs, along with its connected high voltage channels. On the right, the key parameters of the layer's operation is given, along with their associated hardware components.

### Channel View

The lowest layer of the FSM hierarchy is the so called, Channel or Layer View, depicted in Fig. 13, for the MMG



Figure 12: Operational Panels for both MMG and STG subsystems.

and the STG, respectively. There the connected high voltage channel and its model name is displayed in the top. The table contains the key parameters of operation and offers the same functionality as for the quadruplet module view; a trend plot of a variable is called by a right-click in the corresponding cell [10, 11].



Figure 13: Operational Panels for both MMG and STG subsystems.

### Expert Panels

A variety of expert panels (archiving and alarm handling, configuration and check of the periphery address, overall system review, database status, and more) has been developed for both projects, to accommodate all the needs for all type of users (shifter, developer, maintainer, expert) but mainly to facilitate the work of the expert during intervention or debugging and troubleshooting. A typical example of an expert panel, is the colormap, as can be seen in Fig. 14 [10,11]. This panel is developed to provide the controllers a quick overview on the full detector by using color indication. Therefore, 2 wheels are displayed to represent the drift lines for both HO and IP sides. The readout channel are displayed in a colormap matrix (row: sector number, column: pcb num-

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Figure 14: Operational Panels for both MMG and STG subsystems.



Figure 15: The Alarm Screen.

ber) as colorboxes. Via the drop-down menu it is possible to select the layer and the parameter, which should be displayed. These can be parameters of the HV channels as the monitored or set voltages, currents or the environmental parameters of the quadruplets. The color palette is adjusted automatically to the lowest (blue) and highest (red) value, but also can be set by the operator. This allows the operator to determine a layer which is out of the desired range. By hovering the mouse over a layer a tool tip with the numeric value of this layer is displayed. Additionally, by left-clicking on a rectangle a summary of all of its basic parameters is displayed.

#### **ALARM SCHEME**

A powerful alert system (Fig. 15) notifies the operators about detected anomalies/malfunctions of the system during detector operation; providing higher (FSM) and lower (device) level error signalization. Error signalization within the FSM hierarchy is performed using a parallel tree of "Status" objects. For each FSM object, a dedicated Status instance is assigned with the states OK, WARNING, ERROR, and FATAL, signaling a problem in the corresponding part of the detector attributed to one of the following severity: Warn-

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ing, Error, Fatal. An embedded help system also provides instructions required for recovery.

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