CONTROL SYSTEM OF THE SRILAC PROJECT AT RIBF

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Abstract

The RIKEN linear accelerator (RILAC), an injector of the Radioactive Isotope Beam Factory (RIBF) project, was upgraded by installing a superconducting RIKEN linear accelerator (SRILAC) and a 28-GHz ECR ion source (SRILAC project). In addition to controlling these two new apparatuses, the control system of the updated RILAC requires various improvements to the shortcomings of the previous RILAC control system, for example, control methods for electromagnet power supplies using GPIB, a low-performance machine protection system. Moreover, there were issues regarding the integration of small LabVIEW-based systems into the main part of the control system. For efficient operation in the SRILAC project, a distributed control system utilizing the Experimental Physics and Industrial Control System (EPICS) should be adopted in the other parts of RIBF. A higher-level application protocol needs to be integrated into the EPICS channel access protocol. We developed new systems to solve the issues mentioned above and introduced systems that have been proven in other facilities, such as Archiver Appliance as a data archive system. The control system was successfully upgraded and used in the SRILAC beam commissioning completed in 2020. The new control system is currently in its operational phase.

INTRODUCTION

The RIKEN Radioactive Isotope Beam Factory (RIBF) accelerator facility comprises five cyclotrons and two linear accelerators. One of the linear accelerators, the RIKEN linear accelerator (RILAC) [1], has been utilized not only as an injector for cyclotrons but also for stand-alone experiments such as the synthesis of superheavy elements. As an upgrade project, to perform search experiments for superheavy elements with atomic numbers of 119 and higher [2], the superconducting RIKEN linear accelerator (SRILAC) has been introduced downstream of RILAC to enhance beam energy, and a 28-GHz superconducting electron cyclotron resonance ion source (28-GHz SC-ECRIS), similar to the existing RIKEN 28-GHz ECRIS[3], has been introduced at the frontend of RILAC to increase beam intensity [3].

The RIBF control system was constructed using a distributed control system based on the Experimental Physics and Industrial Control System (EPICS) [4]. The new control system for the RILAC upgrade project should be constructed using the EPICS-based control system, and it should be integrated into the existing RIBF control system. The RILAC upgrade project includes various types of hardware such as a 28-GHz SC-ECRIS, beam energy position monitors (BEPM) [5], N2 gas-jet curtain systems [6], and superconducting cavities [7]. Furthermore, the new control system requires improvements to the existing RILAC control system, such as a control method for electromagnet power supplies, a machine protection system, and a data archive system. The protocol for a higher-level application environment should be unified with the EPICS channel access (CA) protocol to enhance operational efficiency. We decided to mainly adopt programmable logic controllers (PLCs) to construct the system and utilize other methods for areas where application of PLCs is difficult considering our limited manpower and resources.

RIKEN 28-GHZ SC-ECRIS CONTROL

The 28-GHz SC-ECRIS was commissioned in advance of the commissioning of other apparatuses. The control system comprises the following: control of ion-source-specific devices (e.g., gas flow controllers, an insertion device of material rods, a high-voltage power supply, and a gyrotron), control of superconducting electromagnet power supplies, and vacuum control [8]. The superconducting electromagnet power supplies embedded MELSEC-Q series as a PLC are connected via NetDev[9], which is an EPICS device support, and controlled by a PC-based EPICS input/output controller (IOC). On the contrary, the control of the ion-source-specific devices and the vacuum control mainly comprised FA-M3 PLCs manufactured by Yokogawa Electric Corporation. These systems have a multi-CPU configuration, a sequence CPU (F3SP71), and a Linux CPU (F3RP61-2L)[10]. Mainly, interlock logic is implemented on the sequence CPU, and EPICS required for higher-level applications is implemented on the Linux CPU.

In contrast to other control systems, some control stations with digital and ana-log modules need to be installed on the high-voltage stage with several tens of kilovolts. Therefore, the connection is insulated between the devices in the high-voltage stage and some devices on the ground level. The control system of the existing 28-GHz SC-ECRIS uses TCP/IP to ex-change interlock signals between

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the safety system and the control stations in the high-voltage stage. To enhance reliability, the new control system uses two different types of CPUs in the main PLC station, which are connected to five PLC substations with star-topology field bus communication using optical fiber [11]. As a result, the interlock signal also exchanges to the control station on the high-voltage stage through field-bus communication using the optical fiber, and the system reliability was improved compared with the system using the TCP/IP-based interlock signal.

MAGNET POWER SUPPLY CONTROL

The introduction of the 28-GHz ECRIS causes a layout change in the low-energy beam transport (LEBT) system, where new power supplies have been introduced to the electromagnets used. In contrast, several old electromagnet power supplies are used for the electromagnets used in medium-energy beam transport (MEBT) systems. The electromagnet power supplies for MEBT use GPIB as the communication protocol for the control system, and their performance is low compared with recent methods such as IP network-based systems. Therefore, we upgraded the control method of power supplies by replacing the GPIB communication with the VME-based method, which is the standard meth-od of the RIBF control system.

In the VME-based method, electromagnet power supplies are controlled by NIO (NIO) system, as in the case of SPring-8 [12]. The NIO system comprises a master board (NIO-C) and a slave board (NIO-S). Optical fibers connect NIO-Ss to an NIO-C inserted in the VME chassis via a branch board. The EPICS IOC in-stalled in VxWorks controls the object by accessing the shared RAM of the NIO-C, and a maximum of 43 NIO-S can be connected to each NIO-C.

For a high-energy beam transport (HEBT) system, old electromagnet power supplies are also used in the new system. Six of these electromagnet power supplies were remotely controlled by GPIB communication, similar to the MEBT system, and no interlock outputs were implemented for the machine protection system described later. As these power supplies were manufactured more than 20 years ago, converting them to the NIO method, as well as the MEBT electromagnet power supplies, has many limitations and is expensive. Therefore, the GPIB communication boards were removed from the MEBT magnet power supplies and the GPIB communication was modified with an easy-to-handle transistor-transistor-logic (TTL) communication by controlling the IO directly with PLC DI/DO.

The controller utilizes a two-CPU module configuration of F3SP71-4S and F3RP71-2L (see Fig. 1). The sequence CPU implements the core of hardware control, such as BIT output, to an electronic substrate, and a strobe signal timing. The Linux CPU module becomes the EPICS IOC and communicates with the man-machine interface to set the current value and provide the status of the electromagnet power supply. In the beam commissioning, approximately 30 modified electromagnet power supplies were controlled via the EPICS CA protocol without GPIB communication.

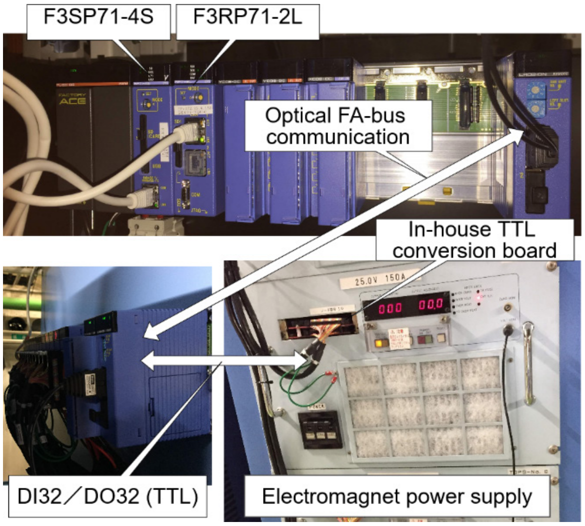

Figure 1: Example of a power supply updated from GPIB to TTL using FA-M3 PLC.

MACHINE PROTECTION SYSTEM

Motivation

In increasing the beam intensity and energy by this upgrade, hardware damage caused by failures of the accelerator components; for example, damage caused by unintended beam orbit changes, will be more serious. As a result, it may cause problems for the beamline components of the HEBT and experimental equipment. In addition, we must prevent problems occurring at the superconducting cavities of SRILAC, such as quenching due to vacuum deterioration caused by beam loss. Therefore, the machine protection system, which is a mechanism to protect the hardware from high-power beams, needs to have a higher performance than before. Before the SRILAC project, the interlock system used in RILAC was realized only via hardware combined with mechanical relays. As a result, the versatility of conventional systems is not high, and hardware circuit modification is required when the input signals are increased, or the logic is changed.

The above-mentioned machine protection system aims to protect hardware from damage caused by beams. In addition, a human protection system is re-quired to secure the radiation safety of individuals involved in accelerator operations and experiments. These two safety systems have different purposes, and systems dedicated to their own purposes should be installed. However, both functions—machine protection and human protection—were implemented in one system, and the wiring and logic were very complicated.

Beam Interlock System

In the RIBF accelerator facility other than RILAC, a beam interlock system (BIS) was introduced in 2006 as a machine protection system. The BIS is a system that stops the beam immediately by exciting a beam chopper that deflects a beam just downstream of the ion sources. The BIS

ISBN: 978-3-95450-221-9 ISSN: 2226-0358 doi:10.18429/JACoW-ICALEPCS2021-MOPV015

also inserts one of the Faraday cups that is pre-assigned according to the position of the trouble. The BIS uses the MELSEC-Q series as the PLCs [13]. The RIBF BIS comprises five stations. Each station has a CPU module (or modules) and is connected to each other by a MELSECNET/H loop configuration for inter-CPU communication.

System Requirements

In developing a machine protection system for the SRILAC project, the following requirements should be fulfilled [14]:

- Avoid as much complexity as possible in both the hardware and software. Human protection and machine protection should be clearly separated.
- The main part of the system logic should follow the RIBF BIS.
- Select hardware that can be maintained for a long time.
- The entire system development and operation process should be completed within our group to enable system modifications and quick troubleshooting.
- A higher-level system will be developed based on EPICS Channel Access (CA), which is the standard control protocol in RIBF.
- A much faster response is required to protect superconducting cavities than the usual response performance achieved by general PLCs.
- The system is scalable, enabling us to accommodate a sudden increase in interlock signals that are urgently required.

Specification

We decided to use FA-M3 PLCs for the BIS of the upgraded RILAC (hereafter, SRILAC BIS). FA-M3 PLCs have been utilized in many RIBF projects [15] and are widely used in safety systems. Because the number of program steps was observed to be large in the prototype, the F3SP76-7S, the most powerful CPU module at the time of system construction, was adopted as the sequence CPU module. The main sequences of the SRILAC BIS were implemented on the F3SP76-7S, a Linux CPU, F3RP71-2L, was also installed as a means of realizing higher-level systems such as the user interface with EPICS, resulting in a multi-CPU configuration.

Communication

The SRILAC BIS avoids the use of inter-CPU communication, and the main unit with the CPU module installed communicates with seven sub-units via an optical FA bus. In this system, the FA bus network is redundantly configured with an optical fiber loop. Based on the cable length and the number of input points, the I/O refresh time of the FA link was estimated to be approximately 110 µs in this configuration.

System Logic

As shown in Fig. 2, various accelerator components and monitors the input interlock signals to the SRILAC BIS and the SRILAC BIS output signals activating the beam chopper switch. Accelerator operators can set the options of the BIS, such as enable/disable interlock, trigger level of analogue inputs, and holding/unholding alarm status for each input signal according to the operation mode. When an anomaly is detected, the chopper stops the beam and inserts the Faraday cup predetermined according to the position of the anomaly.

Table 1: Number of I/O Signal Points Used in the Main Unit and Seven Sub-units of SRILAC BIS. The numbers without parentheses shows the number of I/Os installed and those in parentheses are the number of I/Os actually used as of October 2021.

	Main	#1	#2	#3	#4	#5	#6	#7
DI	56 (36)	56 (41)	32 (29)	32 (32)	32 (28)	32 (17)	32 (10)	0
DO	56 (8)	56 (2)	32 (4)	32 (6)	32 (0)	32 (0)	32 (2)	0
AI	8 (1)	8 (1)	8 (8)	8 (0)	8 (0)	8 (0)	8 (0)	0

I/Os

In general, PLCs can realize a system with a relatively slow response time of a few milliseconds by using standard input modules and transistor output modules (standard I/Os). On the contrary, to realize a system with a response time faster than 1 ms, a field-programmable gate array (FPGA) is selected [14]. In the case of the SRILAC operation, a fast response time is required to stop the beam when triggered by discharges occurring in superconducting cavities. We selected the FPGA-based high-speed IO module (F3DF01: FPIO module) [16] to implement the logic. It has 24 input points and 24 output points as high-speed I/Os with an embedded Xilinx Spartan®-6 LX FPGA. As the logic can be implemented without going through the sequence CPU module, it can be processed in parallel without being affected by the scan time of the program running on the sequence CPU module side. In this system, each input signal of the FPIO module is enabled/disabled via the internal registers of F3SP76-7S. Table 1 lists the number of inputs and outputs used in SRILAC operation.

Performance

The response speed of standard I/O was measured. The conditions were as follows: an interlock signal was input to the F3XD32-3F of subunit #6 at a 100-Hz repetition rate, and the system response time between the input signal and the corresponding output signal to the chopper switch was measured. We confirmed that the system operated at an average of 6 ms. We also measured high-speed I/O. An interlock signal of 100 Hz was input to the FPIO module installed in the main unit, and the time until the output signal to the chopper switch was measured as approximately 78 µs.

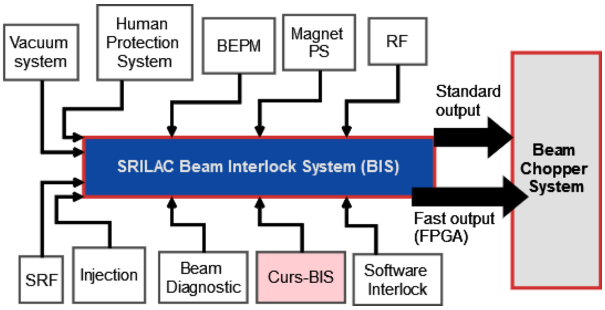

Figure 2: Flowchart of the entire system of machine protection for RILAC operation. The SRILAC BIS is shown as the central blue box. The beam is stopped by the beam chopper by inputting the interlock signals from other systems. There are two outputs—fast and standard.

Curs-BIS

During the SRILAC beam commissioning, a software interlock based on CA was used to detect fluctuations in the excitation currents of the magnet power supplies. Although the software interlock is easy to implement, its reliability and response performance are not high. As the subsystem of RIBF BIS, a beam interlock system driven by a change in current (Curs-BIS) [17] has been developed and used to protect hardware from unintentional changes in the excitation currents of the magnet power supplies. The Curs-BIS has been verified to be effective based on the operation experience of the RIBF BIS up to October 2021, and it has also been introduced to the SRILAC BIS in that all electromagnet power supplies upstream the cryomodules of SRILAC are included. In the near future, Curs-BIS will be installed in all magnet power supplies, including other courses in RILAC.

INTEGRATION WITH SCADA SYSTEM

The MELSEC iQ-R series PLCs are utilized as the controller for monitoring three SRILAC cryomodules, a differential-pumping system, and the readout and settings of the low-level radio frequency (LLRF) system. They work as supervisory control and data acquisition (SCADA) systems. To implement higher-level applications, they should also be integrated into the EPICS.

In the case of EPICS, NetDev as the device support software is adopted to interface the MELSEC iQ-R series with EPICS IOCs, because the MELSEC communication protocol (MC protocol) is a communication protocol with other systems, as in the conventional MELSEC Q series. The IOCs are called virtual-IOCs, which are constructed on a Linux environment with VMware vSphere Standard, and four PLCs for the LLRF system, cryomodules, and the differential-pumping system, are connected to five IOCs, with approximately 5,000 process variables (PVs) in operation.

LABVIEW-BASED SYSTEM

In the control system of the SRILAC project, not only the EPICS IOC running on Linux but also the Windows-based EPICS IOCs are in operation for the BEPM [5] and N_2 gas-jet curtain system [6], and control systems were developed based on LabVIEW. The advantage of the LabVIEW-based system is that the hardware interface is often already provided, and thus development costs can be reduced. On the contrary, LabVIEW-based systems are often operated as two-layer control systems that comprise a PC and devices. We introduced CALab [18] into these LabVIEW-based systems as a SoftIOC, which behaves as a Windows IOC. As a result, these Lab-VIEW-based systems have been successfully integrated into other EPICS-based systems.

HIGHER-LEVEL APPLICATION

Data Archive System

With the number of archived data points expected to increase dramatically owing to the operation of SRILAC, the Archiver Appliance was deployed to improve the data archiving performance [19]. Since 2009, RIBF has been using the RIBF control archive system (RIBFCAS) developed by RIKEN Nishina Center as a data archive system for the data generated by the EPICS IOCs [20]. In contrast, MyDAQ2, developed at SPring-8 as a data store, was also introduced mainly for non-EPICS-based systems [21]. In the RIBF control system, MyDAQ2 is utilized not only as a data store, but also as a method to read data from a non-EPICS-based system through an EPICS CA without EPICS device support software [22]. To realize a user-friendly system for data visualization, the data of RIBFCAS, MyDAQ2, and Archiver Appliance should be visualized on the same system. Therefore, we herein developed a system that implements a Web API to convert RIBFCAS and MyDAQ2 data into the JSON format, thereby making it possible to unify the data format with the Archiver Appliance and display the data with the same viewer software. The maximum data-acquisition cycle was improved to 10 Hz, compared to a cycle of 1 to 20 s in conventional systems.

Operator Interface

To develop the operator interface (OPI) for SRILAC, we use Control System Studio (CSS) as well as MEDM/EDM, which we have been using for a long time. The developed RF control screen for the SRILAC is shown in Fig. 3. In the case of MEDM/EDM, the GUIs are developed on a server installing CentOS7.7, and the developed GUIs are displayed on the screen of each local machine by X11 forwarding. Therefore, the development and execution of the GUIs are performed on the same server. On the contrary, in the case of CSS, running multiple instances on a server is difficult; therefore, CSS is installed separately in each local environment. At this time, we introduced ownCloud [23] as a means of sharing the most recent OPI files with the executors. ownCloud is a system that allows us to introduce online storage such as Google Drive through an intranet and is effective in overcoming the complexity of file sharing using NFS, wherein detailed access control of OPI files to users is difficult.

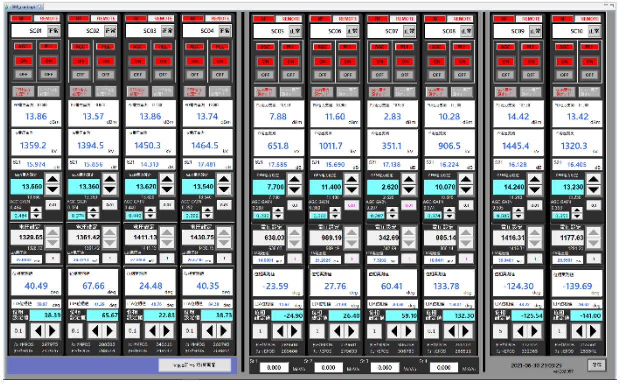

Figure 3: Screenshot of superconducting radio frequency cavities control panel developed by CSS.

CONCLUSION

New control systems have been developed for components newly introduced in the SRILAC project. In addition, several improvements have been made to solve the limitations of controlling the existing components used in RILAC. The development and implementation of the SRILAC BIS were successfully completed. The anomaly signals from all magnet power supplies, RF systems, and vacuum gate valves are input to the SRILAC BIS, and the beam can be immediately stopped to protect the hardware by triggering the beam chopper. The integration of the LabVIEW-based system into EPICS, which had been a serious issue in the past RIBF control system, was also accomplished, and higher-level applications can now be developed in a unified manner using the CA protocol. As a result of these efforts, beam commissioning was successfully completed in 2020.

ACKNOWLEGEMENT

The authors would like to thank Dr. Rok Hrovatin in Cosylab for technical advice with development of the machine protection system.

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