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DEVELOPMENT OF A SINGLE CAVITY REGULATION BASED ON MicroTCA.4 FOR SAPS-TP

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Abstract

A domestic hardware platform based on MTCA.4 is developed for a single cavity regulation in Southern Advanced Photon Source Test Platform (SAPS-TP). A multi-function digital processing Advanced Mezzanine Card (AMC) works as the core function module of the whole system, it implements high speed data processing, Low-Level Radio Frequency (LLRF) control algorithms and an interlock system. Its core data processing chip is a Xilinx ZYNQ SOC, which is embedded an ARM CPU to implement EPICS IOC under embedded Linux. A down-conversion and up-conversion RTM for cavity probes sensing and high-power RF source driver can communicate with AMC module by a ZONE3 connector. A hosted tuning control FPGA Mezzanine Card (FMC) combines both the piezo controlling and step-motor controlling functions for independent external drive devices. The design of the hardware and software of the platform electronics and some test results are described in this paper. Further test and optimization is under way.

INTRODUCTION

The SAPS-TP is next to the China Spallation Neutron Source (CSNS) which is located at Dongguan City, Guangdong Province in China. It is an innovative research platform for advanced accelerator and X-ray technologies serving Southern Advanced Photon Source (SAPS) which will be built as a 4th generation light source based on diffraction limit storage ring, and the CSNS II which is the upgrade of the CSNS. It is mainly composed of a superconducting RF hall, an optical experiment hall, a low temperature hall, a high-accuracy measurement hall and a comprehensive laboratory [1].

The superconducting RF hall is about 3500 m^2. It has 2 vertical test pits and a horizon test station can be applied for assembling and test of the 324 MHz spoke cavity, 648 MHz elliptical cavity, 500 MHz elliptical cavity and 1.3 GHz elliptical cavity, etc.

The function of the single cavity regulation includes amplitude and phase stabilization controlling of cavity field, resonance controlling, continue waveform (CW) or pulse mode conversion and fast interlocking, etc.

MTCA.4 system is the new generation embedded digital hardware platform specifically for high energy physics applications. It is a modular, open standard architecture with high reliability, which is becoming more and more popular, and widely used in European X-ray Free Electron Laser (EXFEL), European Spallation Source (ESS) and Stanford Linear Accelerator Center (SLAC), and so on.

A domestic hardware platform based on MTCA.4 is developed for SAPS-TP single cavity regulation. The system architecture and the development of hardware platform based on MTCA.4 are described in this paper.

SYSTEM ARCHITECTURE

The single cavity regulation for SAPS-TP is mainly used to control to RF field and the resonance frequency of the cavity. The block diagram of the system design is shown in Fig. 1.

Dedicated RF power source (klystrons or solid-state amplifier (SSA)) is used to feed the cavity with required input power. In the RTM module, the forward and reflected power signals, the cavity pick-up signal and the reference RF signal are down-converted to intermediate frequency signals using analog mixers driven by local oscillator signal (LO).

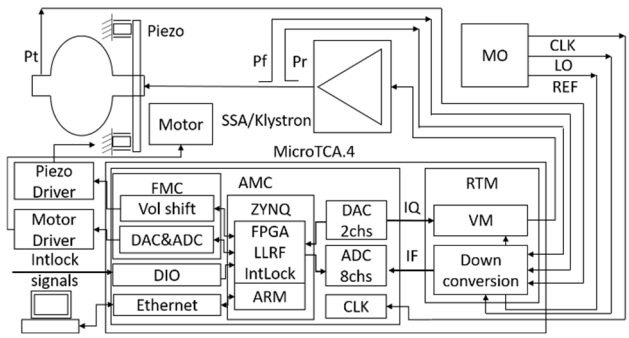

Figure 1: Design of single cavity regulation for SAPS-TP.

The LLRF system implements the cavity RF field controlling feedback loop to keep the RF field amplitude and phase stability [2, 3].

The master oscillator provides RF synchronization signals, such as the reference signal (REF), LO signal and the clock (CLK). In the AMC module, the intermediate frequency signals are sampled by ADCs with the frequency of CLK. Next, the raw data are demodulated to in-phase (I) components and quadrature (Q) components with the IQ or no-IQ algorithm. Errors between setpoint values and detected values are sent to PI controller. The digital I/Q output of PI controller are sent to DACs and are converted to analog I/Q signals. The baseband I/Q signals are then mixed with the in-phase and quadrature-phase components of a REF signal whose frequency is located at the required RF frequency to generate final RF excitation signal. This process is called up-converted which implemented by the vector modulator device of the RTM module.

The superconducting cavity is very susceptible to small changes in dimension, because of its very narrow RF resonance bandwidth. The equipped mechanical tuners can tune the cavity to a resonance frequency. There are two types of tuners, the slow tuners are based on step motors, and the fast tuners are based on piezo elements. The LLRF

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system implement the cavity resonance frequency controlling feedback loop to compensate the cavity detuning caused by reasons such as Lorentz force and microphonics and so on. The digital frequency control output is composed of step motor control signals and piezo control signals. In FMC card, the digital step motor control signals from AMC module are converted to 5 V pulse signals which be sent to step motor driver, and the digital piezo control signals are converted to 0~10V analog signals by ADCs which be sent to piezo driver.

The LLRF system also implement cavity quench detection. The others interlock signals are connected to the digital IO port of the AMC module front panel such as arc, vacuum, temperature, water flow, etc. All the interlock signals are connected to the interlock system which also implemented by the FPGA of the AMC module for fast protection. The RF excitation can be turn off quickly, and the output interlock signal will switch off the RF switchers of the RTM module to cut off the excitation quickly too.

The hardware platform based on MTCA.4 is being developed. It mainly composed of the following devices :

- A domestic AMC module.
- A Module Management Controller (MMC) mezzanine Card.
- A tuning control FMC card.
- A down-conversion and up-conversion RTM module.
- A domestic MTCA.4 chassis including the two 1.6 kW power modules (one for redundancy) and 2 Cooling Unit (CU) modules.

The first version AMC module and the MMC mezzanine card have been produced and tested. The Design of the tuning control FMC card has been finished and is going to be produced. It is based on low speed and high precision DACs and ADCs, and level shift and voltage translation circuit. The RTM module has 8 down-conversion channels and 1 up-conversion channel. It has been developed and produced by the colleagues in the project group. The designed down-conversion RF frequency range is from 300 MHz to 4 GHz, IF frequency range is from 5 MHz to 100 MHz, and up-conversion RF frequency range is from 200 MHz to 4 GHz. Now, its test and optimization of the RTM module is under way. A domestic MTCA.4 chassis including two 1.6 kW power modules and 2 CU modules has been produced by our cooperation manufacturer. Its functional test is finished and the power ripple index need to be improved.

DEVELOPMENT OF AMC MODULE

We developed a domestic multifunctional digital processing AMC module which is shown in Fig. 2. It is expected to be used for vertical and horizontal tests of RF cavity in SAPS-TP, and can also meet the requirements of different systems in CSNS II and SAPS, such as RF system & Control system & Beam diagnostic system.

The AMC module has good compatibility. It is conforming to MTCA.4 standard and the zone3 IO connector assignment class A1.1 CO with double-width mid-size dimensions. The AMC module provide 4-lane PCI Express Gen3 interface connected to port 4~7 of the backplane to realize high speed data transmission with other AMC modules. It also realizes 1GbE Ethernet interfaces (Port 0~1), point-to-point link interfaces (Port 12~15), M-LVDS interfaces (Port 17~20), TCLKA, TCLKB and FCLKA which conform to standard MTCA.4 backplane topology. So, it can work very well as part of a large system based on MTCA.4. What makes it special is that we designed the AMC module and expected that all the digital functions of a single cavity regulation can be finished by one AMC module. So, there is no need to communicate through high-speed serial buses, and the delay of control system is reduced.

Figure 2: Domestic digital processing AMC module.

It has 8 channels ADCs and 2 channels DACs. The Analog Devices AD9268 ADC chip with maximum sampling rate up to 125 MHz and 16-bit resolution is chosen for IF signals sampling. Its analog input bandwidth is 650 MHz, which enable this ADC chips can also be used for 324 MHz or even up to 648 MHz direct sampling applications. A compatible analog front end is designed to adapt to different applications. All the ADC input channels can be configured to AC coupled or DC coupled which be routed to the different differential pairs (TF or PA) of the Zone3 connector conforming to DESY Zone3 class A1.1 CO assignment.

The DAC chip is Analog Devices AD9783. Its dual DA architecture facilitates easy interface to common quadrature modulators. Its sampling rate is up to 500 MHz, and has16-bit resolution. This chip is widely used in CSNS RCS RF system and its performance and stability has been tested.

Because the ZYNQ SOC IO resources is very limited, all the digital interface of AD and DA chip are DDR LVDS interface, so 2 channels can share a group of IO pins.

The core data processing chip is a Xilinx Zynq-7000 SOC system-on-chip. The ZYNQ SOC combines a dual core ARM processor, with a traditional FPGA logic fabric. The single silicon chip can be used to implement the function of an entire system rather than several different physical chips being required. In the single cavity regulation, an EPICS IOC runs in PS part of the SOC which is the ARM processor for remote control, and a LLRF algorithm and interlock system runs in PL part of the SOC which is the FPGA. The data communication between FPGA and ARM

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processor is carried out through AXI bus inside the ZYNQ SOC chip. It simplifies the architecture of hardware greatly, and saves the PCB space which is important to AMC module, because it is not very big.

The Ethernet interface connected to ARM CPU is used for network communications such as remote control and monitoring.

The clock tree is designed to realize the synchronization of signals on board. The clock source can be chosen from the internal crystal oscillator or external input clock signal. There are three input methods for the external clock:

- The front panel clock input.
- The RTM_CLK clock signal from RTM module.
- The TCLKA/TCLKB clock signal from backplane.

The AMC module is designed with ultra-low clock jitter. We expect that the phase error will be smaller than 0.1°, if a 648 MHz direct sampling application based on it.

A 12-channel jitter attenuator SI5394 is used to perform jitter attenuation, and two LTC6950 frequency synthesizer are used for clock distribution. The total theoretical clock jitter is about 170 fs RMS, but not yet be tested due to the unfinished adapter RTM module.

An FMC connector is provided which fully compatible with the FMC Low Pin Count (LPC) standard. It is mainly designed for multi-channel step motor controlling and piezo controlling, and maximally compatibles with commercial FMC boards such as DFMC-AD16 and DFMC-MD22, etc. It is also extended with 3 additional high-speed serial ports of High Pin Count (HPC). So, the interface can also compatible with some usual 4 channel fiber communication FMC card.

The front panel digital IO on LEMO 00 connector has 10 pins and conform to 3.3 V LVTTL standard which can be used for external trigger and interlock signals.

A 4 channels QSFP cage is provided in front panel. And each channel can be used separately for timing, timestamp, interlock signals and optical fiber communication.

This AMC module has 2 GB DDR3 memory size (1 GB memory connected to ARM CPU, 1 GB memory connected to FPGA).

The block diagram of the AMC module is shown in Fig. 3.

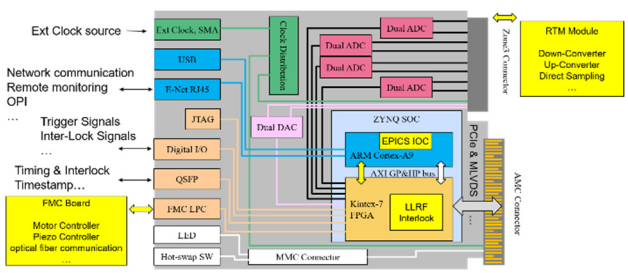

Figure 3: The block diagram of the AMC module.

Because the RTM module is being tested and optimized yet, performance of the AMC module is tested with the compatible signal conditioning input card SIS8900 RTM module and a developed adapter RTM module.

The Fast Fourier Transform (FFT) spectrum of the ADC is shown in Fig. 4.

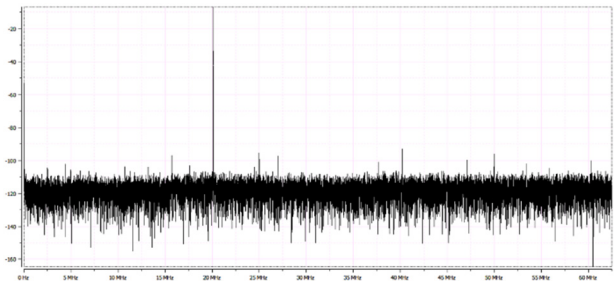

Figure 4: FFT spectrum of ADC.

The results of Signal-To-Noise Ratio (SNR) measurement are from 75.9 dBFS to 76.2 dBFS, and the results of (Spurious-Free Dynamic Range) SFDR measurement are from 86.2 dBFS to 92.1 dBFS.

To test channel isolations, we feed IF signals with different frequencies into the two adjacent channels, and the FFT spectrum of a channel is observed by spectrum analyser. The cross talk signal from the adjacent channel can be observed. The results of the isolation test is shown in Table 1.

Table 1: The Results of Isolation Test

[dB]	Ch0	Ch1	Ch2	Ch3	Ch4	Ch5	Ch6	Ch7
Ch0	-	**76.0**	-	-	-	-	-	-
Ch1	**84.3**	-	**80.9**	-	-	-	-	-
Ch2	-	**75.2**	-	**77.1**	-	-	-	-
Ch3	-	-	**82.2**	-	**80.8**	-	-	-
Ch4	-	-	-	**87.3**	-	**79.5**	-	-
Ch5	-	-	-	-	**78.9**	-	**85.6**	-
Ch6	-	-	-	-	-	**94.8**	-	**85.1**
Ch7	-	-	-	-	-	-	**78.1**	-

We also tested the performance of DAC. The result of SNR measurement is 78.1dB, but there are some bigger harmonic components. The analog circuit behind the DAC output is going to be optimized.

MMC MEZZANINE CARD

The MTCA.4 system provided a remote and centralized health management service for the modules in chassis which is based on the Intelligent Platform Management Interface (IPMI) specification. The MicroTCA management architecture is mainly realized by a MicroTCA Carrier Management Controller (MCMC) and MMC controllers which connect each AMC module to Intelligent Platform Management Bus (IPMB) based on I^2C. MMC controller is a very important part of the AMC module. Without the MMC controller, AMC module will not be detected and identified by MicroTCA system, and the payload power will never be provided for it.

We developed, based on N.A.T NAMC-MMC-Reference Design, a MMC controller mezzanine card for our AMC module. It can be connected to the AMC module by a 40 pins connector. Considering the difficulty and the development time. There are 3 phases of our development:

- Firstly, both the hardware and software are based on the reference design.

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- Secondly, we had developed our own MMC controller software.
- Thirdly, we'll going to design and develop our own MMC controller including all the hardware and software.

We test the MMC controller with the nVent 3U commercial MTCA.4 chassis and NAT-MCH-PHYS80 MTCA Carrier Hub (MCH). Module operational state management, hot swap management, Light-Emitting Diode (LED) management have been tested, and all these functions work very well. The AMC module can be detected and fed with payload power normally. And we also did the voltage sensors and temperature sensors reading test and the temperature threshold event test, all these functions work well too.

The design of MMC controller software is divided to three layers. At the bottom, there is the driver layer including I^2C drivers, voltage sensor drivers and temperature sensor drivers. All the values of sensors are periodically read into a pool which is a list of arrays. The middle layer implements the state machines for module status switching, hot swap management, LED management and threshold event management, etc. The top layer is in charge of IPMI communications including protocol packet parsing and building. This design of software architecture provides many conveniences for debugging and maintenance. So, for MMC testing, a fake temperature threshold event IPMI package can be easily built and send to MCH which will control CU module to increase speed of fans to decrease the AMC module temperature.

The MMC mezzanine card and its test bench are shown in Fig. 5.

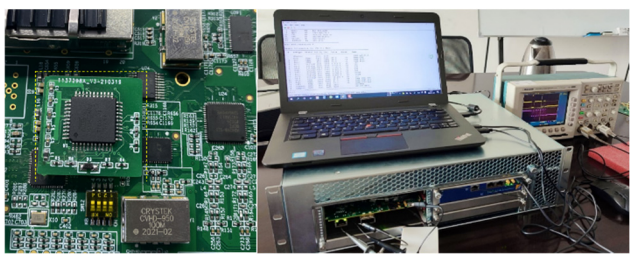

Figure 5: MMC mezzanine card and its test bench.

SOFTWARE DEVELOPMENT

An embedded Linux is developed for the Zynq7045 SOC chip based on open-source Linux kernel source and the Xilinx PetaLinux tools. The experimental physics and industrial control system (EPICS) Input/Output controller (IOC) application Demon is also developed and tested. The Demo of EPICS IOC has 3 types of Process Variables (PVs) which are used to test reading and writing of FPGA registers and reading of waveforms respectively. The data of waveform PV is transferred from FPGA via Direct Memory Access (DMA). A Xilinx AXI DMA intellectual property (IP) core manages and controls the high-speed transmission the data from FPGA to ARM. It be configured to simple mode to fetch data from a FIFO. A user defined IP is developed to control the AXI DMA timing and provide the interface between user data and the Xilinx AXI DMA. The Linux DMA driver for Xlinx AXI DMA is developed based on Xilinx DMA proxy driver which is an open source code and can be download from Xilinx web site. The device support waveform PV realizes the user space operation of DMA based on the Linux DMA kernel module. The entire system including the EPICS IOC demo is no more than 100 MB and can be loaded via a Secure Digital Memory (SD) card for convenient debugging.

SUMMARY

This paper mainly describes the system architecture of the single cavity regulation for SAPS-TP which will be build based on MTCA.4 hardware platform, the hardware and software design and development of platform electronics. The hardware platform has good compatibility and extensible. The developed domestic AMC module provides rich functions and standard extension interface. It is expected to constitute a complete single cavity regulation control system including RF field controlling, resonance frequency controlling and interlock system with the tuning control FMC card and a down-conversion and up-conversion RTM module. There is no need to communicate through high speed serial buses, the system architecture is simplified and the delay of control system is reduced.

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