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THE STATUS OF FAST OBIT FEEDBACK SYSTEM OF HEPS

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Abstract

The new fast orbit feedback (FOFB) system, a typical multiple-input and multiple-output (MIMO) system, is essential for the storage ring of High Energy Photon Source (HEPS). In order to reduce overall latency and achieve more than 500Hz bandwidth, the FOFB system adopt 16 sub-stations with the same hardware and software function to obtain bias-data from the beam position monitors (BPMs) data using 2.38Gbps in the SFPs and send correct-data to the fast corrector power supplies using a serial point-to-point link around the storage ring, and each sub-station share BPMs data with daisy-chained using of 10Gbps in the SFPs. It is optimized to calculate the large matrix based on the singular value decomposition (SVD) taking the digital signal processing (DSP) modules of V7 field programmable gate array (FPGA) with parallel pipeline. For performance tuning and additional flexibility when adding or removing BPMs and fast corrector power supplies, or downloading new matrix, we implement an independent ethernet controller for remote operation. This article presents details on the design and implementation of the FOFB system, and also the future improvements.

INTRODUCTION

High Energy Photon Source (HEPS), a high-performance and high-energy synchrotron radiation source, is one of the major national scientific and technological infrastructures, mainly composing of accelerators, beam lines and experimental stations, supporting facilities, etc, such as show in Figure 1. HEPS will be an original and breakthrough in the fields of basic science and innovative research.

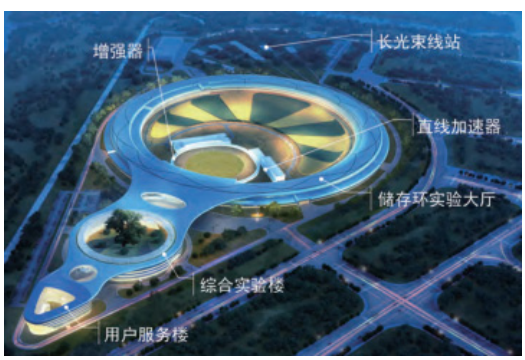

Figure 1: Layout of HEPS.

The size of modern light sources is getting smaller and smaller, and the brightness is getting higher and higher. The performance of the synchrotron radiation photons that finally reach the sample is closely related to the orbital stability of the electron beam. According to the practice of major international laboratories, the stability of the position should be about 10% of the bunch size. For HEPS, the brightest fourth-generation synchrotron radiation source in the world, the bunch vertical emittance should be on the level of 10pm.rad, which corresponds to the vertical bunch size about less than 3μm. Therefore, at the short straight section, the stability of the beam position should be better than 0.3μm.

REQUIREMENT

There are many factors that affect the stability of the beam orbit, including the stability of the magnet power supply, ground vibration, temperature effects, etc. According to ring accelerator physical design and requirements, there are many beam position monitors (BPMs) to monitor the orbit and many correctors to correct the orbit in the storage ring. In order to suppress interference and keep the beam orbit stable, it is we adopt a high-intensity and high-speed orbit feedback system, a typical multiple-input and multiple-output (MIMO)system, to achieve long-term stable operation of the light source based on singular value decomposition (SVD) commonly [1]. The correction algorithm is based on an SVD of the orbit response matrix:

$$\Delta\overline{X} = R\,\Delta\overline{\theta} \quad and \quad R = USV^T$$

$$\Delta\overline{\theta} = VS^{(-1)}U^T\,\Delta\overline{X}. \tag{1}$$

Where $\Delta\overline{X}$ is error that the current orbit is compared to the golden orbit, U and V are matrices whose columns form an orthogonal basis in BPM(X) and corrector magnet θ space, S is the diagonal matrix of singular values. The proportional-integrator (PI) control algorithm operates in this diagonal space and the relevant parameters can be adjusted for each mode separately [2]. All multiplication and calculations stages are done for all eigenmodes at one cycle. Therefore, it is necessary to comprehensively consider the whole time consuming, including the speed of BPMs data acquisition, the delay of global BPMs data distribution and calculation, and other factors. According to accelerator physical design and requirements, the fast orbit feedback system should optimize strategies to achieve the low latency response with BMPs and fast corrector power supplies, which is essential to achieve a certain effective bandwidth range for the stable orbit.

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ARCHITECTURE

The main part of the HEPS is an ultra-low emission electron storage ring, composing of 48 identical hybrid 7BAs cell. According to the accelerator design, there are 12 BPMs and 8 fast corrector power supplies in each cell.

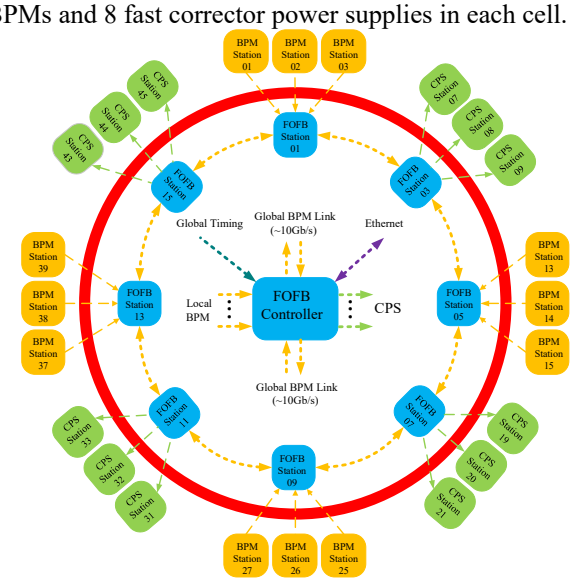

Figure 2: Layout of FOFB architecture.

The storage ring of HEPS, a kilometre scale ring, in order to reduce overall latency and consider feasibility study, we adopt the architecture of daisy-chain based on 16 sub-stations, each sub-station is responsible to interact with local BPMs and fast corrector power supplies. Figure 2 and Figure 3 are shown the layout of FOFB architecture and connection between sub-stations.

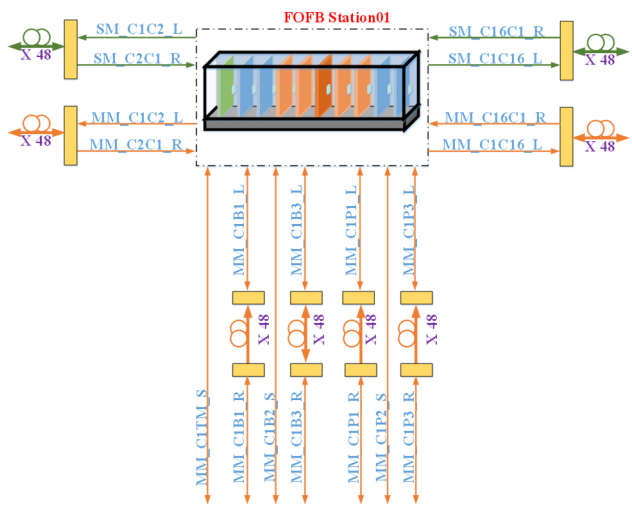

Figure 3: Layout of connection between sub-stations.

Detailly, each sub-station is design and implement to obtain bias-data from BPMs using 2.38Gbps in the SFPs and send correct-data to the fast corrector power supplies using a serial point-to-point link, and each sub-station share BPMs bias-data using of 10Gbps in the SFPs. In order to ensure synchronization with the global beam, all the above working sequence is strictly in accordance with the global clock. For performance tuning and additional flexibility when adding or removing BPMs and fast corrector power supplies, or downloading new matrix, an embedded Ethernet controller is designed as a full hardwired TCP / IP providing internet connectivity to sub-station by using Serial Peripheral Interface (SPI). Figure 4 is shown the hardware architecture of FOFB sub-station.

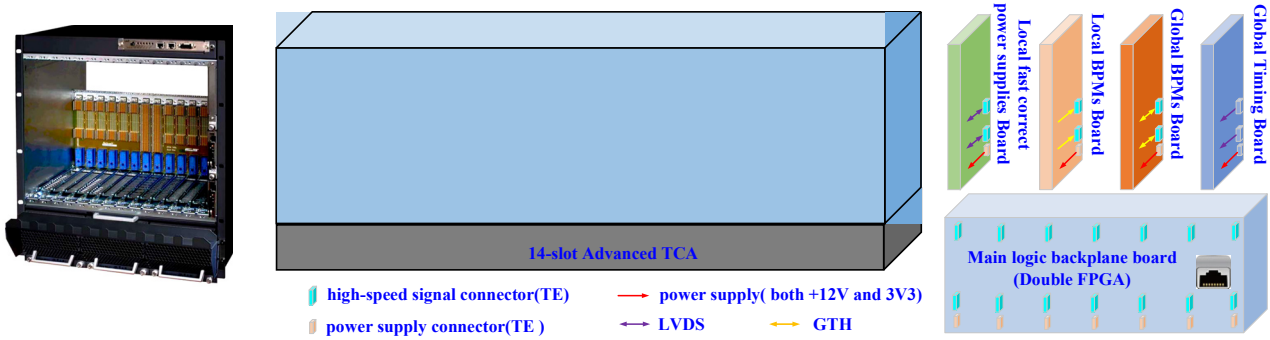

Figure 4: The hardware architecture of FOFB sub-station.

As show in Figure 4, in pursuit of the stable performance with high-speed data transmission, the hardware system of sub-station is only based on ATCA mechanical architecture, but custom the main logic backplane board and the front boards. Furthermore, the sub-station hardware mainly includes:

- 1 main logic backplane board;
- 4 front boards for local BPMs, one of which is reserved for XBPM for beam line;
- 1 front boards for global BPMs;
- 4 front boards for local fast corrector power supplies;
- 1 front boards for global Timing;

The main logic backplane board and the front boards use high-speed TE signal connectors to interact mutually, and providing the front board power supply.

HARDWARE DESIGN

Main Logic Backplane Board

The self-developed main logic backplane board followed the ATCA mechanical size is one of the core board of FOFB. Considering the stability and reliability for long-term operation and future upgrade, the backplane of FOFB is adopt a large-capacity, high-density architecture, as

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shown Figure 5. We have completed the whole schematic and PCB design, including:

- FPGA chip: Xilinx/XC7VX690T;
- High-speed: 80 channels of GTH transceiver @10Gb/s (3 front boards@16 channels for local BPM data collect, 1 front boards@16 channels for global BPM data transmission);
- Clock: embedded timing / on-board 100MHz crystal clock / LEMO clock output;
- LVDS: 14 slots @20 channels;
- Ethernet: W5500iso;
- Power: +12V power supply.

… …

A total of 22 layers (thickness 2.8mm) of the main logic backplane board PCB are preliminarily drawn up, as shown in Figure 7, which is divided into signal layer and plane layer:

(1) Signal layer:
Top/L3/L5/L7/L9/L14/L16/L18/L20/Bottom, the thickness of copper foil is 0.5oz;

(2) Plane layer:
L2/L4/L6/L8/L10/L11/L12/L13/15/L17/L19/L21, the thickness of L10, L11, L12, L13 copper foil is 2oz used for 1V@100A power supply rail and GND, other lays are all 1oz.

Note: FPGA and other modules are mainly placed on the top layer, which faces the rear of the chassis.

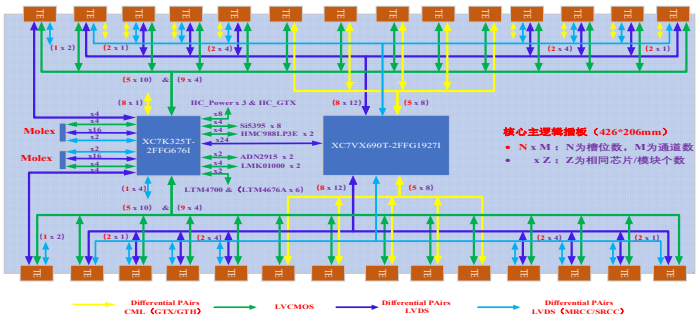

Figure 5: The diagram of signal flow.

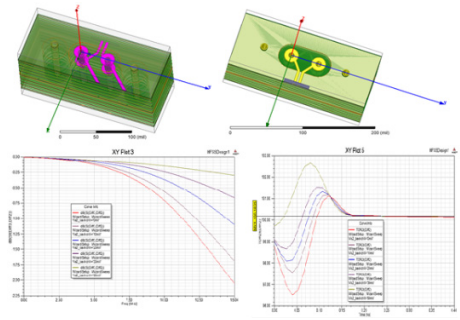

Figure 6: The diagram of via simulation.

Via acts as conductors (PCB) in connecting traces on different layers. In the case of low frequencies, via will not affect signal transmission. However, as the frequency increases (above 2.5 GHz) and the rising edge of the signal becomes steep, via cannot be only simply regarded as a function of electrical connection, but must be carefully considered for signal integrity, which appear as breakpoints with discontinuous impedance on the transmission line, causing signal reflections, as shown in Figure 6.

The power distribution network (PDN) characterizes the change of load size and load frequency, as shown in Figure 8. Its parasitic parameters must be small enough to ensure that in a certain frequency range to ensure that the power supply voltage meets the working voltage range of the load under the maximum current scenario. However, the voltage of the load transmitted by the PDN is no longer equal to the output of the power supply. Once the voltage obtained by the load is lower than the working demand of the load, it will cause unpredictable failure of the load. When the steady-state current of the load reaches a certain value, the supply voltage of the power supply meets the working voltage range of the load, which is the low frequency part of the PDN.

The FOFB main logic backplane is designed with multiple independent chips based on the IIC or SPI bus. In order to monitor the operating status of the chips in real-time, it is necessary to read the operating parameters and measured information through the interface of a FPGA chip, released by ethernet timely. IIC or SPI bus mainly includes 5 parts: the fast corrector power supply front board, the local/global BPMs data front board, the core main logic backplane and the ATCA slot, all of which have been design detailed.

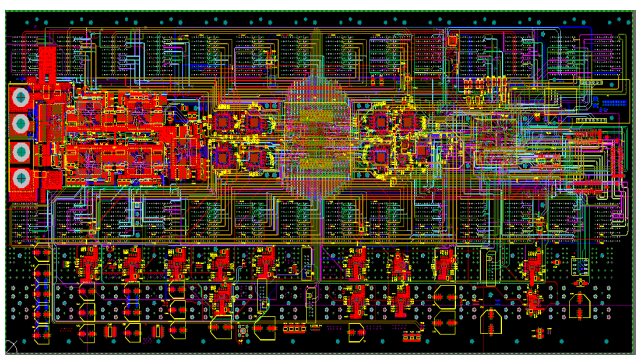

Figure 7: The diagram of PCB.

Target Impedance	Units	Value
Supply Voltage (Min)	V	1
I max	A	100
Transient Current	%	50
Vripple (+/-)	%	5
Frequency target	MHz	250
Ztarget = ΔV / ΔI	Ω	0.0010

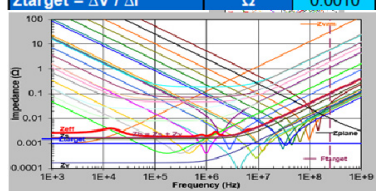

Figure 8: The diagram of capacitance simulation.

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Front Board

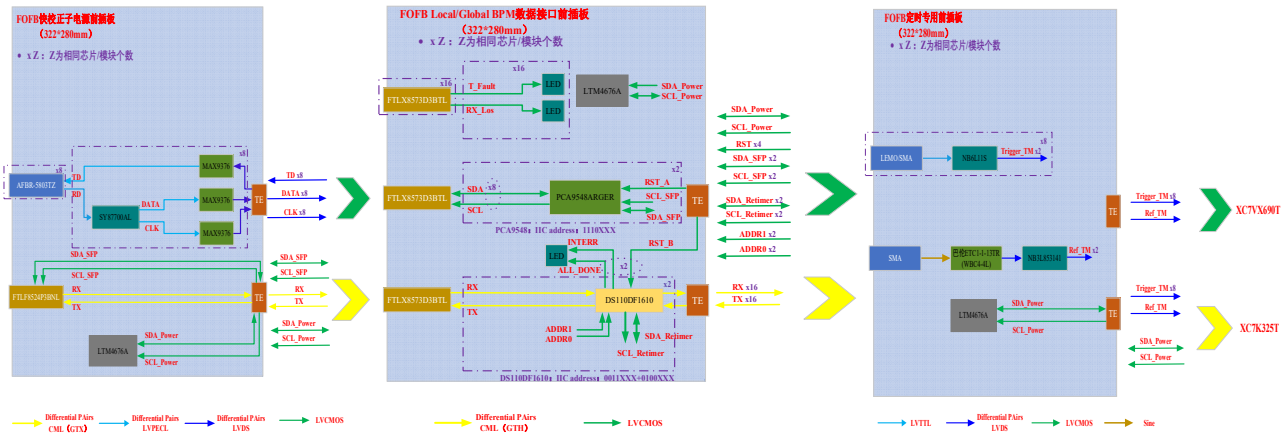
Figure 9 is shown the diagram of signal and function of the front board.

The fast corrector power supply front board is mainly responsible for outputting current settings for power supply substations, and the data transmission rate is about 50Mb/s.

The local BPMs data front board is mainly responsible for collecting 3*12 groups of 32bit effective data, the rate is about 2.38Gb/s. The global BPMs data front board is mainly responsible for transmitting the BPMs data collected by this substation to the global BPMs data transmission link, and where is obtained other FOFB substations, and the rate is about 9.5Gb/s.

The local BPMs data front board and the global BPMs data front board adopt the same hardware based on the ATCA standard (322mm*280mm).

The dedicated timing front board is mainly responsible to receive the timing trigger signal and reference clock signal from global timing and sent to the main logic backplane board. The FOFB system is controlled by the 22kHz timing signal, reset signal, system synchronization start signal, system synchronization stop signal, and loop injection signal sent by the timing system.



(a) (b) (c)

Figure 9: The diagram of signal and function of the front boards.

LOGIC DEVELOPMENT

Data Calculation Module

The data arithmetic module adopts a pipeline design, which is advantage that it can accurately control the data to reach a certain position at a certain time and reduce the delay at the same time, as shown in Figure 10.

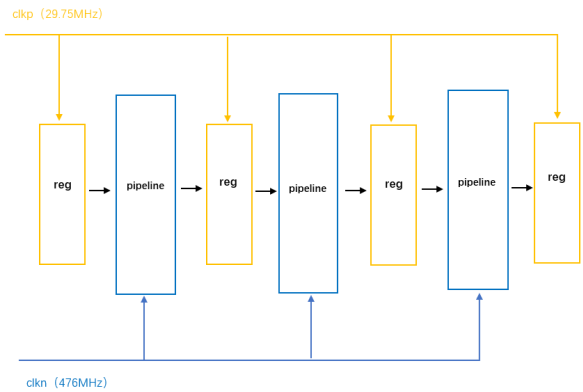


Figure 10: The diagram of pipeline design.

Data Storage Module

Because the amount of parameter data that the system needs to store is very large, so it is necessary to call the Block Memory resource in the FPGA for data storage. Considering the design goal of FOFB low latency, BRAM is used in the memory module design to ensure that the data is written and read in one clock cycle to reduce latency.

CONCLUSION

In order to reduce the system response time as much as possible and improve the effective feedback bandwidth of the FOFB system, we propose a new hardware architecture that can quickly obtain all BPMs data in the storage ring, and quickly complete large data calculations, and send the setting to the fast corrector power supply in real-time. It is shown that the architecture can achieve an effective bandwidth of more than 500 Hz, which also meets the main requirements of the HEPS project.

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