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STATUS OF THE uTCA DIGITAL LLRF DESIGN FOR SARAF PHASE II

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Abstract

One of the crucial control systems of any particle accelerator is the Low-Level Radio Frequency (LLRF). The purpose of a LLRF is to control the amplitude and phase of the field inside the accelerating cavity. The LLRF is a subsystem of the CEA (Commissariat à l'Energie Atomique) control domain for the SARAF-LINAC (Soreq Applied Research Accelerator Facility – Linear Accelerator) instrumentation and Seven Solutions has designed, developed, manufactured, and tested the system based on CEA technical specifications. The final version of this digital LLRF will be installed in the SARAF accelerator in Israel at the end of 2021. The architecture, design, and development as well as the performance of the LLRF system will be presented in this paper. The benefits of the proposed architecture and the first results will be shown.

INTRODUCTION

The SARAF-LINAC project intends to accelerate proton and deuton beam currents from 0.4mA to 5mA up to 40MeV for deutons and 35 MeV for protons. To achieve this, the field in the cavities needs to be controlled and regulated. The LLRF is the device in charge of maintaining the cavity gradient and phase stability in presence of beam. Seven Solutions has designed and implemented the LLRF system including all the hardware, gateware (FPGA code) and software needed to fulfil the specifications derived from [1]. The LLRF channels required for the SARAF-LINAC phase II [2] will drive both normal conducing cavities and superconducting cavities.

The factory acceptance tests (FAT) results will be detailed in this paper.

SPECIFICATIONS

The LLRF must be able to regulate the cavity field both in pulsed mode and in continuous wave (CW). From the simulations and studies performed in [1], the main LLRF system requirements were derived. They are listed in Table 1. The frequency of the full accelerator is 176MHz. This is the reference frequency for the LLRF system.

Table 1: LLRF Requirements

Requirement	Value
Operation frequency range	176MHz +/-100KHz
LLRF delay	< 1us
Input amplitude RMS error	< 0.03%
Input phase RMS error	< 0.03º
Output amplitude stability	< 5%
Output phase stability	< 5º

HARDWARE

The LLRF HW is based on the uTCA.4 technology. The system is composed by two boards (Fig. 1):

The LFE (LLRF Front End) is in charge of conditioning the RF inputs signals to interface them to the ADCs. In addition, the RF drive outputs are amplified and filtered in this board.

The AMC (Advanced Mezzanine Card) digitizer controller board includes all the components (ADCs, DACs, PLL, FPGA, DDR memory…) needed to perform the acquisition and generation of the RF signals as well as all the digital signals processing to implement the different algorithms and features included in a LLRF system. The design based on a FPGA provides the system with a great flexibility making it capable of being adapted to the requirements of different accelerator facilities and to be placed on a rack or in a single standalone mode.

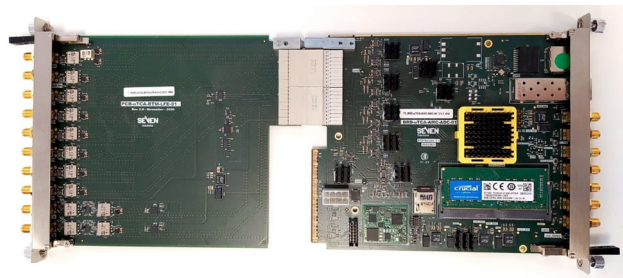

Figure 1: LLRF HW composed of LFE and AMC boards.

The HW is designed to have two LLRF channels making possible to control two cavities with one set of board. Each channel generates one RF drive signal (Uamp) and monitors three RF signals (Fig. 2):

- Ucav: Cavity voltage.
- Uci: Incident voltage.
- Ucr: Reflected voltage.

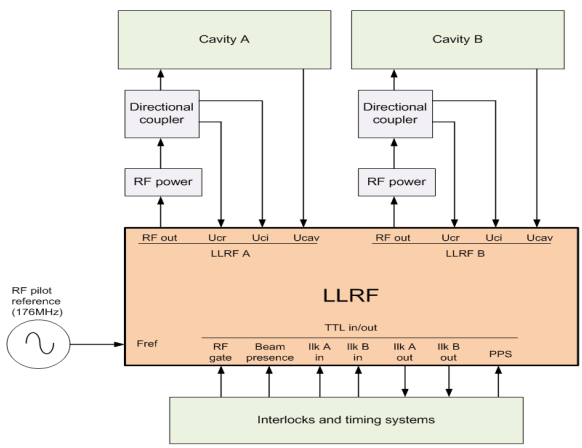

Figure 2: LLRF block diagram.

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GATEWARE

The LLRF system is based on SoC technology. A Zynq UltraScale FPGA from Xilinx has been used in the design. This family of FPGAs combines a great amount of programmable logic and two dual core ARM processors in the same chip, offering enough resources and flexibility to implement all the functionalities that characterize a LLRF system.

A block diagram with the main gateware elements is shown in Fig. 3.

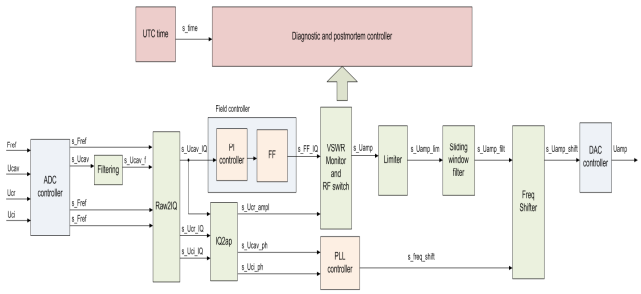

Figure 3: Gateware architecture block diagram.

The LLRF system can operate both in pulsed mode and in continuous wave. Moreover, it can operate in opened loop for conditioning and in closed loop for cavity regulation.

The main functionalities implemented in the FPGA are:

- ADC controller: In charge of configuring the ADC chips and acquiring the RF samples from them.
- Demodulation: To get the IQ component of the RF signal form the ADCs.
- Calibration: Used to compensate gain and phase offsets in the acquired RF signals.
- Field controller: Composed by a PI (Proportional-Integral) controller, to maintain stable the amplitude and phase of the cavity field, and a feedforward controller to compensate the beam loading effects.
- VSWR monitor: To monitor the reflected voltage and shut off the RF generation in case this voltage exceeds a configurable limit.
- Limiter: To prevent from generating undesired high RF output levels.
- Sliding window filter: To perform pulse shaping over the RF output pulses.
- Freq shifter: Used to cause a frequency displacement over the RF output signal.
- PLL controller: Allows to track the cavity resonant frequency automatically when the LLRF is operating in opened loop.
- DAC controller: Responsible for configuring the DAC chips and sending the data to be converted to analog domain.
- Diagnostic and post-mortem: The systems store the value of the RF signal as well as other internal signals of interest and the status of the system in the DDR memory. These data are used for displaying in real time some information. In addition, postmortem files are generated, in case of alarm, which allow the operator to investigate the causes of the alarm and to know the status of the LLRF at that time.

EMBEDDED SOFTWARE

Figure 4 illustrates the main architecture developed on the Zynq UltraScale to provide the functionality and communications required for the control system installed on the LLRF system.

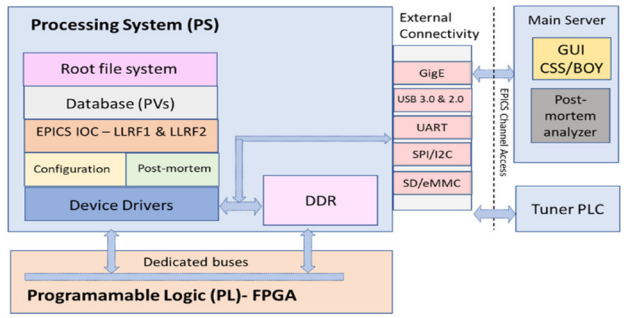

Figure 4: Software architecture.

The presented architecture consists of:

- Operating system: generated using the open-source tool Buildroot. Generates a single image to be loaded on the board contain the Linux kernel image, root file system, BOOT.bin (FPGA image), device tree and uboot.
- Low level drivers: allows the communication between the control system layer and low level devices. Communication between FPGA, DDR memory and I2C/SPI devices, such as EEPROM, are part of the drivers included in the embedded software.
- Control system layer: allows the communication between the low level drivers and the EPICS Channel Access. EPICS based is used in this development, and more specifically, AsynPortDriver is used as interface to the EPICS Channel Access (CA). Records and PVs are defined to access to the different elements defined to monitor and control the LLRF.

OPERATOR INTERFACE

The operator interface is implemented in CSS (Control System Studio) and Python. It enables the user to easily control the system making used to the interface provided by EPICS with the process variables (PV). Figure 5 is an example of how to control tasks such as monitoring, settings and display of PVs on a very easy way.

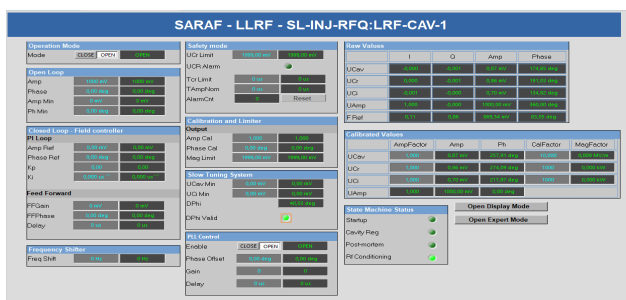

Figure 5: Graphical user interface.

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FAT TESTS RESULTS

In this section, some of the main tests performed in Seven Solutions laboratories are described.

Output Jitter

The jitter is directly related to the system stability. During the FAT, the jitter of the output signal Uamp has been measured. Figure 6 shows that the LLRF system has a very low additive jitter. The output jitter is 182fs when operating with a frequency reference source with 112fs of rms jitter.

Figure 6: LLRF output jitter.

Stability in Opened Loop

The RF output stability has been measured for amplitude and phase for 15 minutes. The measures have been taken when the LLRF operates in opened loop. The results are shown in Table 2.

Table 2: Output Stability

Magnitude	Value
Amplitude stability	0.014%
Phase stability	0.315º

Stability in Closed Loop

The stability in closed loop has been measured keeping the LLRF operating in closed loop during 48h. In Fig. 7 it can be seen the amplitude and phase of Ucav and the temperature fluctuation during the test. The results can be found in Table 3.

Table 3: Stability in Closed Loop

Magnitude	Value
Amplitude stability	0.066%
Phase stability	0.034º

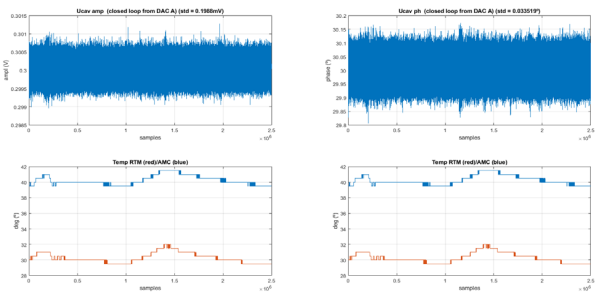

Figure 7: Long-term stability in closed loop.

Precision in Opened Loop

The precision in the acquisition of the input signal has been measured. For an input signal of 0dBm, the data acquired for the three inputs (Ucav, Uci and Ucr) have been stored during 300ms. The precision in amplitude and phase is shown in Table 4.

Table 4: Precision in Openend Loop

Magnitude	Value
Amplitude precision	0.03%
Phase precision	0.022º

Precision in Closed Loop

To measure the precision in closed loop the LLRF systems is connected in loop, that is, the output Uamp is connected to the input Ucav. With the system operating in closed loop (keeping the Ucav voltage in amplitude and phase to the values configured from the interface as setpoint), the output Uamp is stored and processed to get its stability.

As it is a precision measure, the capture is performed over a short period of time, in this case 1.2ms. The results are shown in Table 5.

Table 5: Precision in Closed Loop

Magnitude	Value
Amplitude precision	0.04%
Phase precision	0.018º

Loop Delay

One of the requirements was that the total loop delay of the LLRF system must be less than 1us. This delay is a measure of the response time of the PI controller when a disturbance occurs in the cavity field. To measure this, the LLRF is connected in loop and operating in closed loop. During the test, the proportional constant Kp of the PI controller is set to a value that causes the loop to diverge. In Fig. 8 can be seen the steps caused by the action of the PI controller. The length of these steps is the time the LLRF takes to perform an action when the measured signal (Ucav) changes. The measured response time is 912ns.

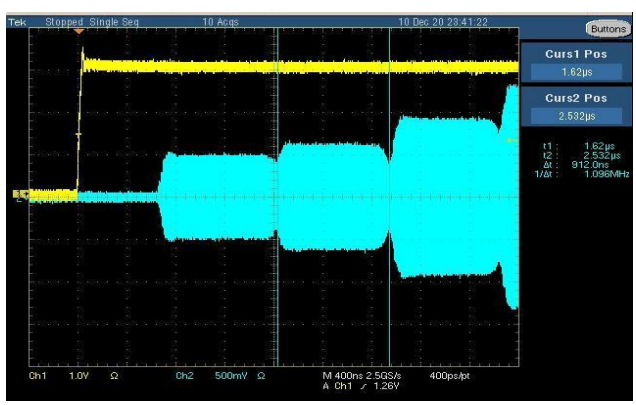

Figure 8: Loop delay test.

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Functional Tests

Several functionality tests have been carried out to check the different features that the LLRF systems implements.

A 176MHz bandpass filter with high Q factor (13000) has been used to test some features in conditions like those when the LLRF is connected to a cavity. In Fig. 9 it can be seen the LLRF regulating the voltage when the RF output (Uamp) is connected to the bandpass filter and the filter output is connected to Ucav. The LLRF is operating in closed loop and pulsed mode (RF gate in pink in the figure). In yellow we can see Uamp and in blue Ucav (the output of the bandpass filter).

The feedforward capability has been also tested during the FAT. In Fig. 10 it is shown RF gate signal in blue and the beam presence gate signal in yellow. As the LLRF is no connected to a cavity and there is no beam, it is observed how the Ucav signal increase its level, with the rising edge of the beam presence gate signal, but immediately the PI loop compensate this increase. In the same way, when the feedforward stops having effect, Ucav suffers a level drop that is quickly compensated by the PI controller.

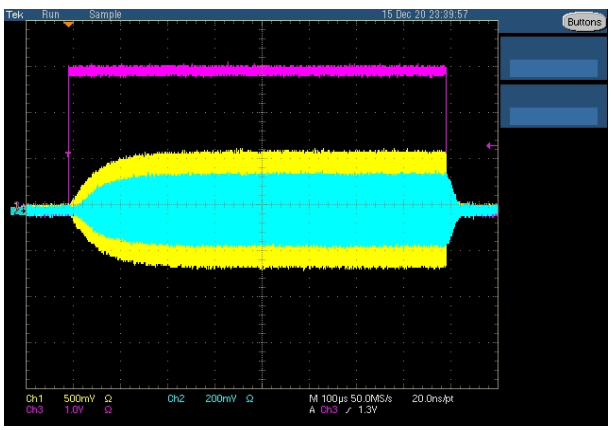

Figure 9: LLRF Ucav regulation test.

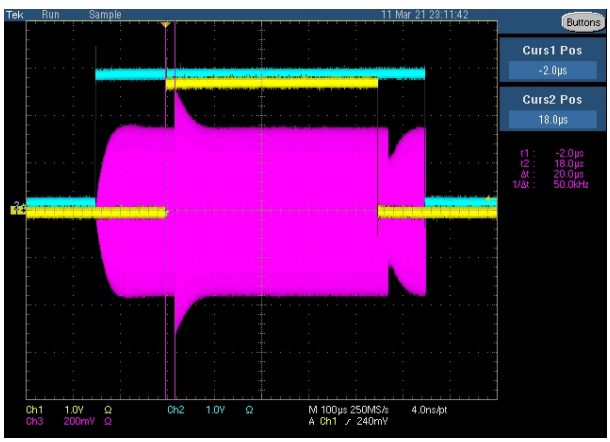

Figure 10: Feedforward capability test.

One of the most interesting functionalities of the LLRF system is its PLL functionality. Thanks to this functionality, the LLRF can track, when operating in opened loop, the resonant frequency of the cavity.

Two measurements of the filter phase characteristic were done separately. The first test, blue curve in Fig. 11, is the following: the incident voltage (Uci) and the output frequency of the LLRF are fixed. The transmitted voltage (Ucav) is measured (in mV), as well as the phase shift between Uci and Ucav. It gives a first graph of the phase as a function of the transmitted voltage for different frequencies. Then, instead of fixing the frequency, we did a second test by fixing the phase between Uci and Ucav. The PLL should lock to the frequency that provides the phase. This is the red curve in Fig. 11. In principle, if the PLL locks to the phase as expected, red and blue curves should be identical. This is precisely what was measured, validating the PLL function.

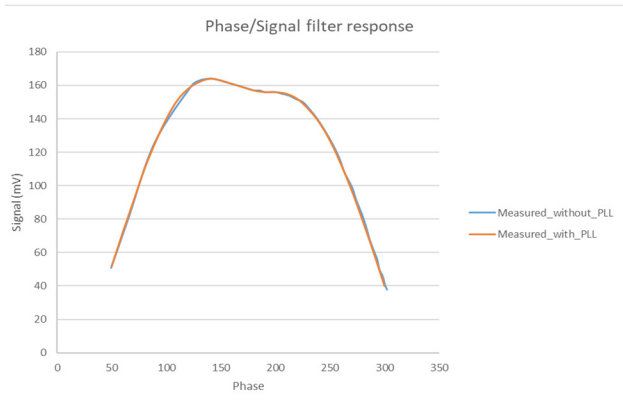

Figure 11: PLL functionality test.

CONCLUSIONS

This paper presents the LLRF system for SARAF project phase II designing and manufactured by Seven Solutions according to the specifications given by CEA. The FAT tests have ben satisfactory, and the next step will be the integration of the LLRF systems (18 resulting in a total of 36 channels) in the SARAF facilities in Israel.

REFERENCES

[1] L. Zhao, G. Ferrand, F. Gougnaud, R. Duperrier, N. Pichoff and C. Marchand, "Status of the LLRF system for SARAF project Phase II", arXiv:1909.12562 [physics.acc-ph] (2019).

[2] N. Pichoff, D. Berkovits, R. Duperrier, G. Ferrand, B. Gastineau, F. Gougnaud, M. Jacquemet, J. Luner, C. Madec, A. Perry *et al.*, "The SARAF-LINAC Project 2019 Status", in *Proc. IPAC'19,* Melbourne, Australia, May 2019, pp. 4352-4355, doi:10.18429/JACoW-IPAC2019-THPTS116