ISBN: 978-3-95450-221-9 ISSN: 2226-0358 doi:10.18429/JACoW-ICALEPCS2021-WEPV033

ARCHITECTURE OF A MULTI-CHANNEL DATA STREAMING DEVICE WITH AN FPGA AS A COPROCESSOR*

J. M. Nogiec†, P. Thompson, FNAL, Batavia, IL 60510, USA

Abstract

The design of a data acquisition system often involves the integration of a Field Programmable Gate Array (FPGA) with analog front-end components to achieve precise timing and control. Reuse of these hardware systems can be difficult since they need to be tightly coupled to the communications interface and timing requirements of the specific ADC used. A hybrid design exploring the use of an FPGA as a coprocessor to a traditional CPU in a dataflow architecture is presented. Reduction in the volume of data and gradual transitioning of data processing away from a hard real-time environment are both discussed. Chief design concerns, including data throughput and precise synchronization with external stimuli, are addressed. The discussion is illustrated by the implementation of a multi-channel digital integrator, a device based entirely on commercial off-the-shelf (COTS) equipment.

INTRODUCTION

One of the typical dilemmas designers face when building a system is whether to buy or build its components. This also applies to test and measurement systems used in High Energy Physics. Readily available, so-called commercial off-the-shelf (COTS) components are ubiquitous and can reduce development cost and offer product support by manufacturers. Unfortunately, the offered instruments or modules may not be precisely what is needed. A solution can be to build an instrument in-house, but from available COTS subcomponents, as is the case for the digital integrator device discussed in this article.

Construction of a multi-channel streaming integrator from COTS subcomponents is presented in the context of using an FPGA as a coprocessor in order to provide predictable and guaranteed data processing performance. The discussed integrator is functionally extensible, thus it has been named the Extensible Digital Integrator (EDI).

Digital integrators have been very successful in testing accelerator magnets, and they are crucial parts of rotating coil systems and single stretched wire systems, the cornerstones of the measurement toolset used in this domain.

FPGA AS COPROCESSOR

A Field Programmable Gate Array (FPGA) allows engineers to design and program data acquisition and control hardware to cater to the specific needs of their applications. Typically, systems employ FPGAs as controllers of hardware and signal preprocessors or conditioners. In these architectures, the FPGA is positioned between the I/O and the higher layers of data processing or control (see Fig. 1a).

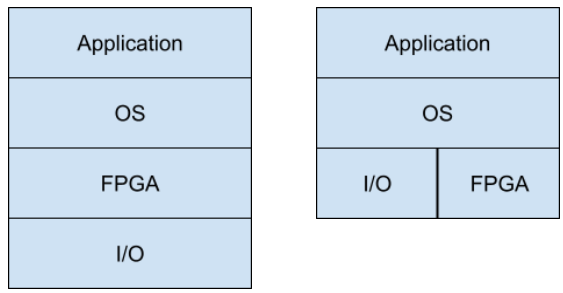

Figure 1: Layers in the system using an FPGA: a) for signal acquisition, b) as a coprocessor.

Another typical application of FPGAs is as a coprocessor offloading computationally intensive functions from a main processor. This solution offers deterministic performance in demanding data processing situations, especially in real-time applications (see Fig. 1b).

The EDI combines both of these hardware organizations into a single architecture. Here, the FPGA serves as both a coprocessor integrating signals and a real-time signal processor acquiring external triggering signals.

The performance of the analog-to-digital converters in dedicated PXI coprocessor modules is inadequate for our needs, and there is no access to the selected DSA ADC boards directly from the FPGA. These factors contributed to some design specifics of the EDI solution.

INTEGRATORS

Digital integrators have proven to be useful in building test systems to measure magnetic fields in accelerator magnets. In fact, they are often a crucial instrument in systems based on the rotating coil and single stretched wire techniques.

These instruments integrate input signals (voltages) over time intervals provided by internal or external triggers, such as a train of pulses or the output of an angular encoder. Historically, these systems evolved from voltage-to-frequency converters connected to up-down counters and trigger boxes [1, 2] to systems using analog-to-digital converters coupled with DSP coprocessors performing integration [3-8]. More recently, FPGAs have offered a very attractive alternative to other integrator hardware

* Work supported by the U.S. Department of Energy under contract no. DE-AC02-07CH11359
† nogiec@fnal.gov

ISBN: 978-3-95450-221-9 ISSN: 2226-0358 doi:10.18429/JACoW-ICALEPCS2021-WEPV033

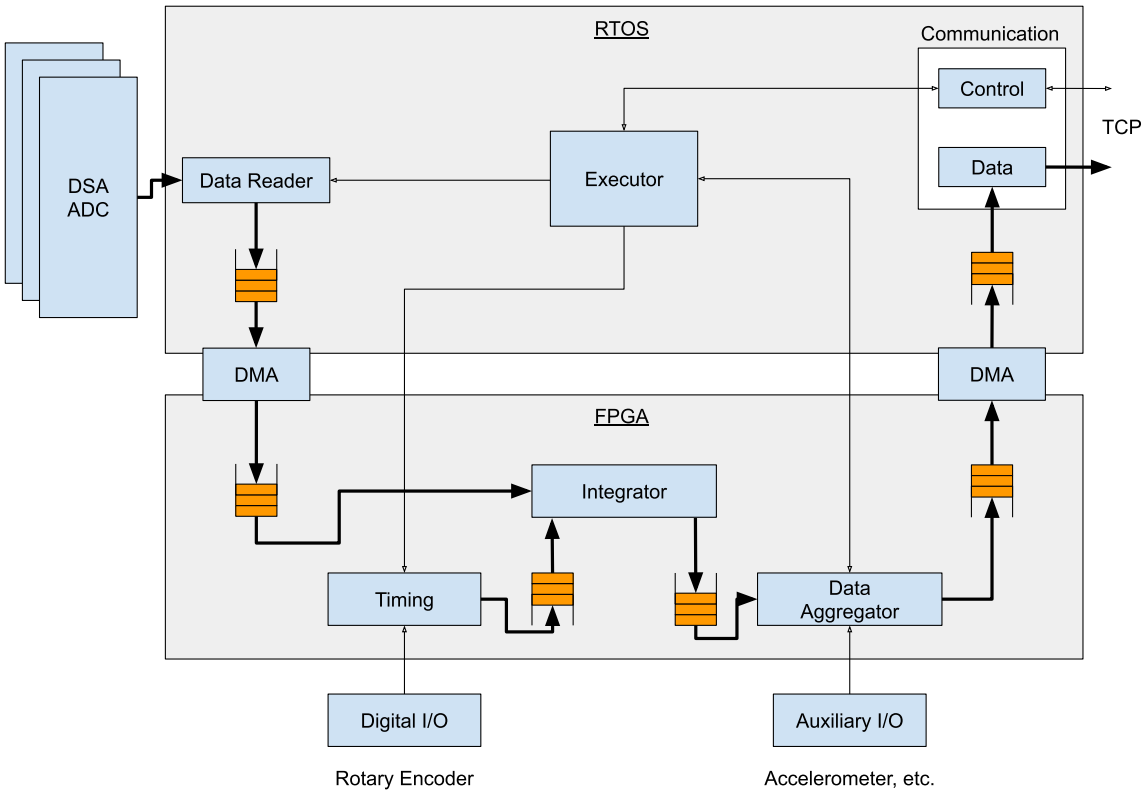

Figure 2: Organization of the EDI.

solutions, allowing for both acquisition of signals and signal processing [9, 10].

EDI HARDWARE

The EDI uses an FPGA for acquisition of external timing signals and a PXI bus for acquiring data from a set of analog-to-digital converters. Both the ADCs and the FPGA come as COTS PXIe modules produced by National Instruments Corporation.

FPGA

The PXIe-7856 reconfigurable I/O module featuring a Xilinx Kintex-7 FPGA provides ample logic area for creating integration and data processing algorithms. Memory space for queues is supplied in part by its 11,700 kbits of block RAM [11]. When used with a compatible PXIe chassis, these FPGA cards as well as the ADC cards will automatically synchronize with the 100 MHz chassis backplane clock with less than 250 ps of skew between modules [12]. Therefore, the ADC sampling clock and the 40 MHz FPGA clock used for keeping time between encoder triggers are derived from the same time base, which effectively eliminates clock drift between the modules.

Additionally, some ancillary functions (e.g., accelerometer readings for probe orientation monitoring) are provided by some built-in 16-bit successive approximation register (SAR) ADCs [13].

ADC

The PXIe-4464 ADC cards are members of the Dynamic Signal Acquisition (DSA) family of modules from National Instruments. With programmable gains and good frequency domain performance, these cards are well suited for harmonics measurement applications. The sampling rate is also adjustable, with a maximum of 204.8 kS/s. A CMRR of up to 105 dBc (depending on selected gain) provides adequate noise rejection on long probe cable runs. Samples are provided by a delta-sigma ADC with a resolution of 24 bits [14].

However, one potential drawback of this card is that it is not compatible with peer-to-peer streaming, necessitating the routing of sample data through the RT controller (adding some overhead) before it can be sent to the FPGA.

EDI ORGANIZATION

The programmatic implementation of the EDI includes software in the real-time operating system (RTOS) layer and firmware in the FPGA layer (see Fig. 2). Both the software and firmware are built as a set of collaborating modules communicating via queues.

Commands directing the operation of the EDI come via a TCP connection and are encoded by the control and communication module and are then sent to the executor module. The executor module keeps the state of the integrator and orchestrates the operation of other software and firmware modules.

ISBN: 978-3-95450-221-9 ISSN: 2226-0358 doi:10.18429/JACoW-ICALEPCS2021-WEPV033

The input data reader module starts data acquisition in the ADC channels and reads the incoming data, which subsequently are sent via a DMA channel to the FPGA where they are appended to the raw data queue.

At the same time, the timing module starts to read the triggering signals and for each trigger appends an element to the timing queue. The element contains the time elapsed from the previous trigger (integration time).

The integrator module reads an element from the head of the timing queue, calculates the number of ADC samples to integrate, performs integration, and appends the results of integration and integration time to the integrator output queue.

Depending on the configuration, a given number of elements in the integrator output queue are combined in the data aggregator module and sent via a DMA channel to the RTOS layer.

The integrated and aggregated data are received by the RTOS and are passed to the data communication module, which send them via a channel in the TCP-based connection to the consumer of the data.

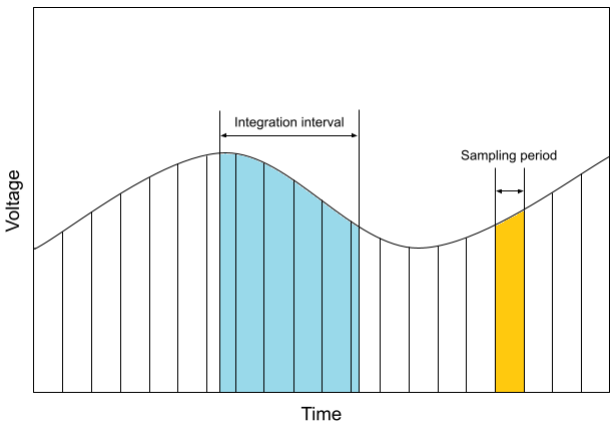

Figure 3: Integration interval and ADC sampling time.

INTEGRATION

The process of integrating signals over a given period of time is conducted in the FPGA. In this process, the samples from a given time interval are added up. The signals/pulses that trigger the starting and stopping of each integration interval come asynchronously to samples produced by the analog-to-digital converters. This necessitates the inclusion in the integration calculations the fractions of the first and last sample in the integration window (see Fig. 3). The beginning and end of each integration window is calculated using the sampling frequency and the integration time. The integrator module maintains a timeline for the sequence of samples that allows it to determine the number of samples (with the precision of a fraction of a sample) to be removed from the input queue and summed up.

The triggering information and the integration timeline are common to all data channels and the same operations are performed on each signal channel for each integration window. The original raw data stream is significantly reduced in size due to this integration process.

The implementation of integration has been conducted while paying close attention to the precision of calculations.

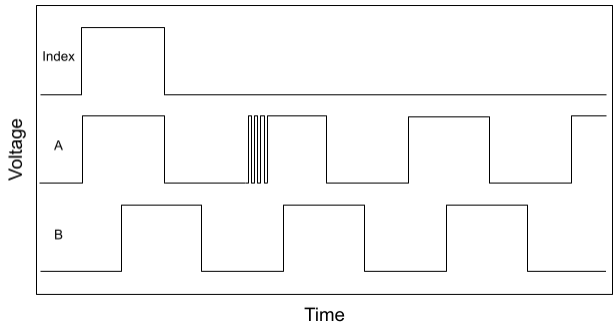

Figure 4: Sample angular encoder signals. Note noise example on A signal.

TRIGGERING

There are two main types of integrator triggering: internal and external.

Internal triggering relies on the FPGA clock to specify integration windows. The clock ticks are counted and after a required number is reached a new element is added to the timing queue.

External triggering is based on monitoring digital inputs for changes in their levels. A simple version will use a single digital input, providing a train of pulses controlling integration intervals. A more complex method, normally used in rotating coil measurement systems, is to trigger using angular encoder signals (see Fig. 4). Here, three signals are monitored to detect changes of their levels: index, A, and B. The A and B signals have their phases shifted, therefore allowing for detection of rotation direction. A, B, or a combination of both are used for generating timing triggers. The index pulse allows for starting the integration process at a known angular position (index position).

In practice, the external triggering signals may be distorted, which may lead to improper operation of the integrator. One problem is associated with vibrations of the mechanical parts attached to encoders, which may result in detecting multiple closely coupled triggers (see Fig.4). To eliminate such problems, the timing module ignores any trigger occurring too close to the previous trigger. The timing module also counts the number of triggers in each full revolution, index-to-index, and compares with the expected number.

A second problem has to do with spikes produced by noise in angular encoder signals that can be detected as “false” triggers. Multiple probing is used to eliminate these disturbances. In essence, whenever a rising edge is detected on a trigger line, the inter-trigger time is saved to a temporary register (in units of 40 MHz clock ticks) and a small debouncing delay is started. If the trigger line still reads as logic high by the end of this delay, then the inter-trigger time is validated and is placed on the queue. Counting then restarts using this debouncing delay period length as a starting point instead of zero, since this delay

ISBN: 978-3-95450-221-9 ISSN: 2226-0358 doi:10.18429/JACoW-ICALEPCS2021-WEPV033

period has elapsed after what would have been the reset-to-zero condition for the time counter. Otherwise, if the trigger line returns to a logic low state, then the contents of the temporary register are discarded and time-counting continues to increment.

With this method, false triggers can be ignored without introducing any phase drift to the inter-trigger times. This debouncing delay is user-settable and is determined through empirical observation since noise conditions at different test stands can be unique.

EDI INTERFACE

The EDI is controlled via an Ethernet interface. Commands and data are sent through the same multichannel socket connection with separate channels devoted to streaming data and exchanging control messages. This basic functionality can be extended by adding additional channels devoted to transmission of auxiliary data and their control information.

On the client side, applications use the provided set of commands to communicate with the EDI. A subset of commands that captures the core functionality of the EDI includes:

- CONFIG: a command that sends a cluster of settings of various EDI properties and parameters,
- RUN: a request to start streaming of integrated data from all configured ADC channels,
- ABORT: a command used to stop the streaming of data (typically, the EDI is configured to send only a discrete number of integrated samples),
- TEMPERATURE: a command that reads the temperatures of all ADC modules, which can be used to correct results or check operating conditions,
- ACCELEROMETER: as an example of specialized commands added to tailor EDI functionality to a specific application, this is a request to read auxiliary analog inputs connected to an accelerometer

Depending on the configuration selected, the EDI may either perform integration using a discrete number of triggers, or it may run in a continuous mode. In this continuous mode, the EDI will not stop streaming integrated data until an abort command is received. In either mode, data is never saved to disk on the EDI but is instead always sent over the network, allowing for potential further processing of the data by other consumers on the network.

PERFORMANCE

The are some performance limitations inherent to the organization of the EDI. The integration time is provided with a resolution limited by the FPGA clock. Also, over a longer period of time, the timeline calculations will introduce additional errors due to their limited computational precision. Therefore, over a very long continuous integration measurement run (measured in hours), operations need to be periodically restarted to eliminate accumulation of errors and avoid a substantial phase shift.

Having two separate clocks in the system, with one used by the ADCs and another in the FPGA for inter-trigger timing, could also adversely impact the performance of the EDI. To address this very problem, both clocks have been synchronized.

The performance of the EDI is also strongly dependent on the performance of the ADCs, their time and temperature stability, offset, noise level, and dynamic range, among other factors.

EXTENSIBILITY

The EDI device has a configurable number of ADC integration channels with a minimum of 4 channels and has been tested with 8, 12 and 16-channel configurations. Access to additional digital and analog I/O modules allows for the instrument to also serve some auxiliary functions.

One example is the extension to read accelerometers developed for the rotating coil system for the HL-LHC AUP project [15]. The available auxiliary analog input channels are read via the FPGA and data are sent to the consumer via a separate communication channel.

Another extension developed for the same measurement system allows for receiving a stream of real-time readouts of magnet current obtained from a DCCT and distributed in the measurement hall via a fiber optic connection. This implementation uses the auxiliary digital inputs to create a receiver of encoded data packets in the FPGA.

As a future extension, the authors plan to include drift compensation and discrete Fourier transform calculations in the FPGA, therefore allowing for the conversion of integrated signals to a frequency spectrum.

SUMMARY

Building instruments from COTS parts is an attractive alternative to buying devices that don't necessarily fulfill all the requirements or building complex instruments in-house. It offers shorter development cycles, lowers development costs, and produces a device fully suited to the task.

The Extensible Digital Integrator (EDI) is an example of successfully combining several COTS hardware component and, by adding software and firmware, creating a powerful and specialized test instrument.

The EDI employs an FPGA mainly as a coprocessor, but also for synchronizing acquired analog data with external timing signals. It can be further extended to acquire and process other signals via the auxiliary I/O on the FPGA.

The use of an FPGA not only as a signal preprocessor, but as a coprocessor, can also be applied in other situations in real-time systems where data needs to be processed with hard real-time constraints.

The described digital integrator is fully functional and the conducted performance tests and comparisons with other available integrators show its satisfactory performance. In a multichannel configuration of 16 ADC channels it is capable of continuously processing 4096 triggers per second.

ISBN: 978-3-95450-221-9 ISSN: 2226-0358 doi:10.18429/JACoW-ICALEPCS2021-WEPV033

REFERENCES

[1] B. Brown *et al.*, "A V/f-based waveform recording system for magnetic measurements", DESY-HERA Report 87-23, 1987.

[2] P. Galbraith, "Portable digital integrator", CERN Internal Technical Note 93-50, AT-MA/PF/fm, Jan. 1993, http://cdsweb.cern.ch/record/1362025/files/Portable_Digital_Integrator_1993.pdf

[3] P. Arpaia *et al.*, "A fast digital integrator for magnetic field measurements at CERN", in *2006 IEEE Instrumentation and Measurement Technology Conference Proceedings*, 2006, pp. 67-71. doi:10.1109/IMTC.2006.328175

[4] P. Arpaia, A. Masi, and G. Spiezia, "A digital integrator for fast and accurate measurement of magnetic flux by rotating coils", in *IEEE Transactions on Instrumentation and Measurement*, vol. 56, no. 2, Apr. 2007, pp. 216-220. doi:10.1109/TIM.2007.890787

[5] P. Arpaia, V. Inglese, and G. Spiezia, "Metrological characterization of an improved DSP-based on-line integrator for magnetic measurements at CERN", in *2007 Instrumentation and Measurement Technology Conference Proceedings*, 2007, pp. 1-5. doi:10.1109/IMTC.2007.379251

[6] P. Arpaia, L. Bottura, L. Fiscarelli, and L. Walckiers, "Performance of a fast digital integrator in on-field magnetic measurements for particle accelerators", in *Review of Scientific Instruments*, vol. 83, no. 2, Feb. 2012, paper 024702. doi:10.1063/1.3673000

[7] *Fast Digital Integrator FDI2056 User's Manual*, Metrolab, May 2014, https://www.metrolab.com/wp-content/uploads/2015/07/FDI2056_manual_v20_rev12.pdf

[8] G. V. Velev *et al.*, "A fast continuous magnetic field measurement system based on digital signal processors", *IEEE Trans. Appl. Superconductivity*, vol. 16, no. 2, Jun. 2006, pp. 1374-1377. doi:10.1109/TASC.2005.869702

[9] P. Arpaia, U. Cesaro, and P. Cimmino, "Enhanced fast digital integrator for magnetic measurements", *Review of Scientific Instruments*, vol. 88, no. 8, Aug. 2017, paper 085103. doi:10.1063/1.4996539

[10] X. Wang *et al.*, "A hybrid data acquisition system for magnetic measurements of accelerator magnets", Lawrence Berkeley National Laboratory, 2012, https://escholarship.org/uc/item/4gh4w163

[11] 7 Series Product Selection Guide, 2014, https://www.xilinx.com/support/documentation/selection-guides/7-series-product-selection-guide.pdf

[12] Synchronization Explained, Jun. 2021, https://www.ni.com/en-us/support/documentation/supplemental/10/synchronization-explained.html

[13] NI PXIe-7856 Specifications, Dec. 2016, https://www.ni.com/pdf/manuals/378000b_02.pdf

[14] NI PXIe-4464 Specifications, Dec. 2016, https://www.ni.com/pdf/manuals/376165b.pdf

[15] J. M. Nogiec *et al.*, "Designing a Magnetic Measurement Data Acquisition and Control System with Reuse in Mind: A Rotating Coil System Example", submitted to the 27th International Conference on Magnet Technology, Fukuoka, Japan, Nov. 2021.