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THE FAST PROTECTION SYSTEM FOR CSNS ACCELERATOR

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Abstract

The CSNS (China Spallation Neutron Source) consists of an 80 MeV H^- LINAC, a 1.6 GeV Rapid Cycling Synchrotron, two beam transport lines and one tungsten target and three beam lines. The designed proton beam power is 100 kW in Phase-I [1]. The fast protection system plays an important role to guarantee the safe operation of accelerator. The response time requirement for the CSNS fast protection system is less than 10 µs. The design of CSNS FPS was based on FPGA technology, and the VME bus and SFP connector was adopted for the hardware design. Different beam interlock and mitigation logic was designed so as to fulfil the operation requirements.

INTRODUCTION

CSNS accelerators are designed to accelerate very high intensity proton beam, Fig. 1 shows the schematic layout of the CSNS facility. The uncontrolled beam loss may permanently damage or give a high radiation dose to the accelerator components along the beam line [2, 3]. Therefore, high reliability for machine protection system is the basic requirement. The accelerator protection system must be carefully designed so that we can avoid the unnecessary beam loss. Besides, the availability, scalability, maintainability and the budget were also need to be carefully considered in the design and implementation stage.

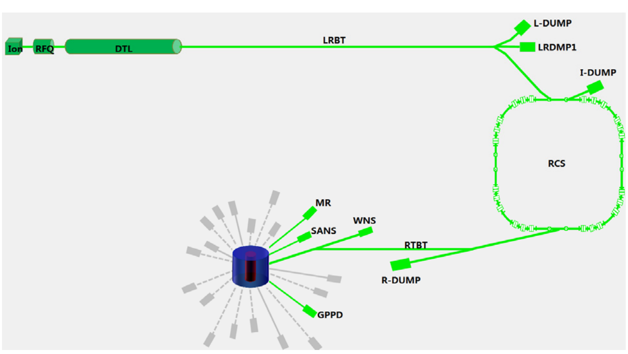

Figure 1: Schematic diagram of CSNS.

CSNS accelerator protection system consists of two protection systems, one is the PLC based slow protection system: NMPS (Normal Machine Protection System), the other is the FPGA based FPS (Fast Protection System). The response time within 20ms and 10µs are required for NMPS and FPS respectively [4]. The overall protection systems for CSNS as shown in Fig. 2. The output signals of PPS (Personnel Protection System) and TPS (Target Protection System) are input into the two NMPS main stations. RMS (Run Management System) can be seen as the beam permit system. Three beam stopping actuators are designed for protection system, which including ion source timing, post acceleration power supply of ion source and RFQ power source.

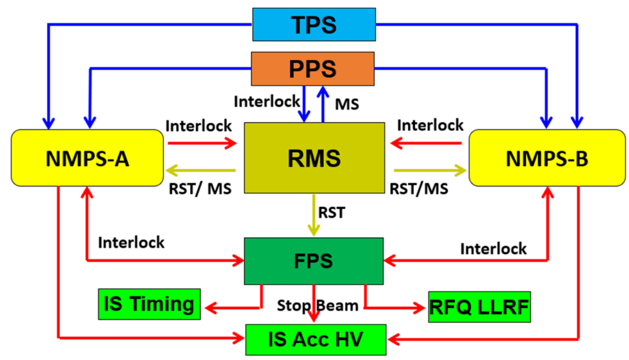

Figure 2: Relations among the protection systems for CSNS facility.

OVERVIEW OF THE CSNS FPS

The FPS for CSNS accelerator was designed based on the FPGA, the hardware was designed in VME form. In order to unify the hardware type, two kinds of boards were designed, one is the main logic board as shown in Fig. 3, the other is the optical signal input board as shown in Fig.4.

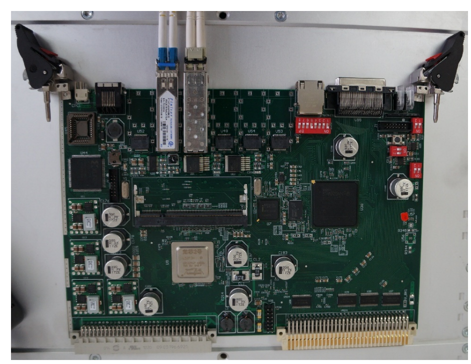

Figure 3: Picture of the FPS main logic board.

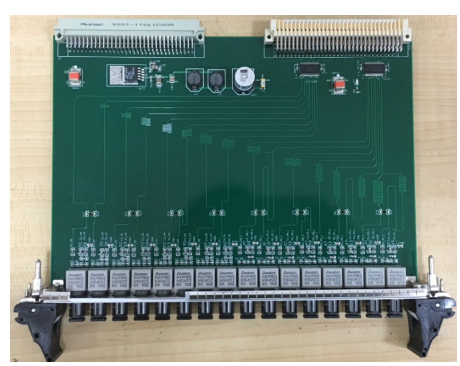

Figure 4: Picture of the FPS signal input board.

The high-speed serial communication technology was adopted by the main logic board, and the common plastic

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optical connector was utilized by the signal input board. The main logic board can be programmed to perform different function, which can be used for signals convergence or the beam interlock.

The tree topology was adopted by the FPS. In the actual deployment, FPS consists of three layers, the signal input layer, the signal convergence layer and the beam interlock layer. Figure 5 shows the topology diagram of the FPS.

The FPS consists of one beam interlock station, two signal convergence stations and several signal input stations. The beam interlock station is responsible for carrying out the shutdown of beam or mitigation measures. The signal input stations are distributed near the corresponding devices. The total number of input signals is 304, and the signals are from DTL power supplies, beam loss monitors and Linac RF system.

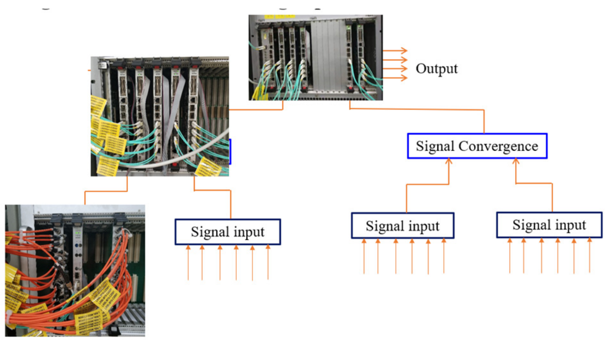

Figure 5: Diagram of the FPS topology.

BEAM INTERLOCK LOGIC

The input signals of FPS from different devices has different type. For example, the over threshold signal from beam loss monitor is in pulsed type, the fault signal from power supply will be in high level state. So, according to different input signal type, different action will be carried out by FPS. The following will introduce the detail of the interlock logic and actions.

Logic of Mitigation

For the pulse input signals, the mitigation measures will be carried out by FPS. When FPS receives pulsed signal, it will generate the output to inhibit next 1 second beam. Figure 6 depicts the output logic of inhibiting next 1 second beam. Figure 7 shows the details of mitigation actions, FPS will switch off the timing triggers to ion source and RFQ power source for 1 second, and after 1 second, the timing triggers will back to normal so that the beam will be recovered automatically.

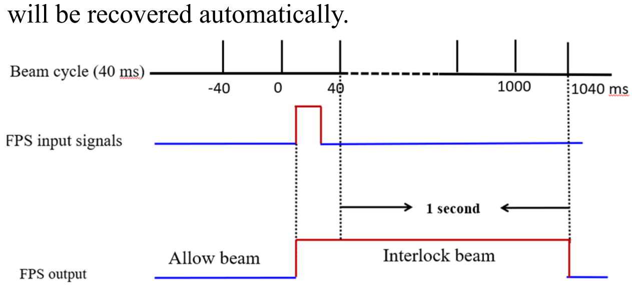

Figure 6: The logic of inhibiting the next 1 second beam.

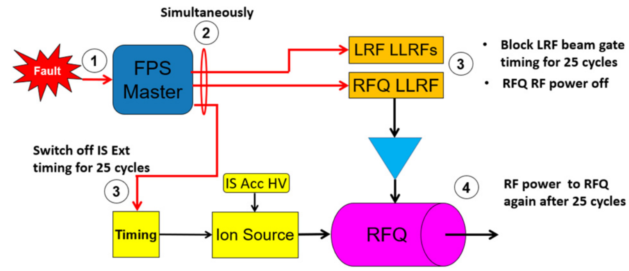

Figure 7: Actions of mitigation measure.

Logic of Shutdown of the Beam

Figures 8 and 9 show the logic of how the latched output is generated by FPS. When the FPS receives the fault signal, the mitigation measure will be taken place firstly. If the during time of fault signal is more than 5 seconds, or there are two pulsed inputs in 5 seconds, the output of FPS will be latched. The shutdown of the beam actions will be taken place.

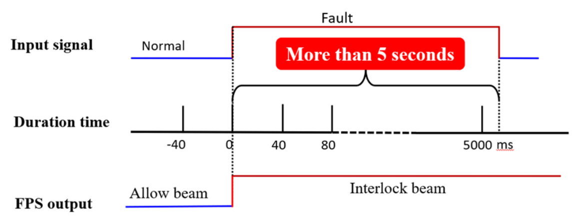

Figure 8: The latched output logic for PS input.

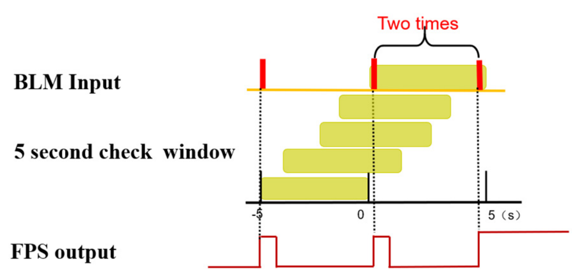

Figure 9: The latched output logic for BLM input.

Figure 10 show the detailed actions of shutdown of the beam. If the output of FPS changed to latched state, FPS will send interlock beam signals to MPS and ion source acceleration power supply, then the machine status will be changed to BEAMOFF and the ion source acceleration high voltage will be switched off. In this case, the manual beam recover process should be carried out in order to resume the beam.

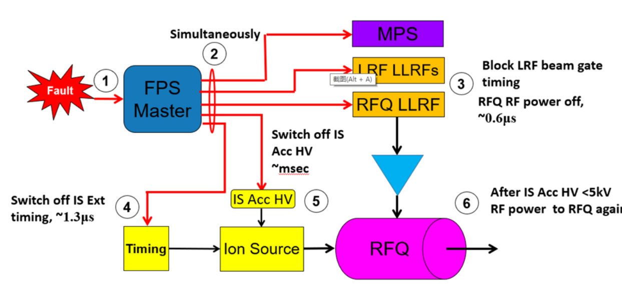

Figure 10: Actions of shutdown of the beam.

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CONCLUSION

The fast protection system for CSNS accelerator has been put into operation for more than three years. Different beam interlock logic was designed to fulfil the operation requirements. The fast protection system runs smoothly and reliable. The hardware will be upgraded in the CSNS-II project.

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