

DEVELOPMENT OF FPGA-BASED BUNCH-BY-BUNCH BEAM CURRENT MONITOR*

C.S. Liu, Qing Luo, B.G. Sun, Z.R. Zhou[#]

NSRL, University of Science and Technology of China, Hefei, Anhui 230029, P. R. China

Abstract

Bunch-by-bunch (BxB) beam current measurement is an important method to study filling pattern of injection and beam instability threshold for multi-bunch operation storage ring, also, necessary equipment for top-up injection. A high-speed high-precision ADC and FPGA are used to construct the bunch-by-bunch beam current measurement system. FPGA reads data from ADC, and transfer the data to PC via USB. A LabVIEW program is running on PC to process the data, and communicates with other accelerator equipment with EPICS by CA Lab. Besides the bunch-by-bunch beam current measurement, the BxB longitudinal tune is measured by the system, and other potential bunch-by-bunch beam diagnostics study could be done in future, like bunch-by-bunch beam life etc., to improve the performance of the storage ring of Hefei light source.

INTRODUCION

HLS-II is upgraded by 2014, a synchrotron light source with a storage ring of circumference of 66.13 meters [1]. After upgrade, HLS-II consists of an 800MeV linac and an 800MeV storage ring with 8 dipole bend magnets, 32 quadrupole magnets and 32 multi-function sextupole magnets. The storage ring has 8 straight sections, one for injection system, one for RF system, and the other 6 straight sections are for insertion devices. The main parameters of the storage ring are listed on table 1.

Table 1. Parameters of the HLS-II storage ring

Injection energy	800MeV
Operation energy	800MeV
Circumference	66.13 m
Current	>300mA
RF frequency	204.030 MHz
Harmonic number	45
Revolution frequency	4.534 MHz
Life time	>5 hours

Current BxB beam current monitor system [2] of HLS-II is based on a high-speed digital oscilloscope (Agilent MSO7104), with 4GS/s 8bit sampling rate, to get BxB beam current. A FPGA-based BxB beam current monitor is developed to simplify the system architecture

and to improve the precision of measurement. The system design and commissioning results are presented in this article.

THE ARCHITECTURE DESIGN

The FPGA-based beam current monitor system uses fast ADC to sample the sum signal of BPM with peak voltage, with sampling rate of RF frequency of storage ring, and PFPGA read the ADC data into FIFO, then transferring the data to PC. A LabVIEW program is running on PC to finish the BxB data analysis.

The whole BxB beam current monitor system consists of a button-type BPM, a power combiner, a low-pass filter, an ADC sampling board, an FPGA board and a PC, and the system scheme is shown as figure 1.

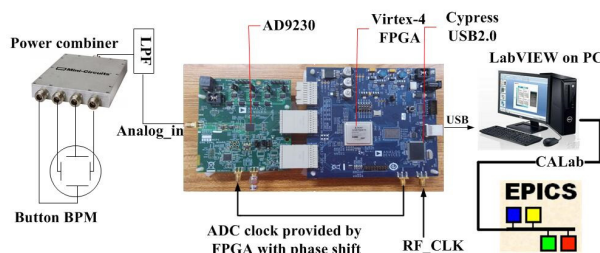


Figure 1: Overview of BxB beam current monitor system.

Power combiner is a 4-way splitter/combiner, ZFSC-4-1 of Mini-circuits, with 1MHz-1000MHz bandwidth. Low pass filter is VLFX-780 of Mini-circuits, with DC-780MHz bandwidth. ADC is AD9230 from ADI, 12 bit resolution with 250MHz top sampling rate, with 700MHz analogue bandwidth. FPGA is XC4VFX20, Virtex-4 of Xilinx.

Peak Sampling of Sum Signal of BPM

The electrons in a bunch of a storage ring are usually expressed with a Gaussian distribution:

$$I_b(t) = \frac{eN}{\sqrt{2\pi}\sigma_\tau} \exp\left(-\frac{t^2}{2\sigma_\tau^2}\right) \quad (1)$$

Where σ_τ is bunch length, N is the number of electrons. And the sum signal of a button type BPM could be expressed as:

$$V_\Sigma(t) = \frac{keNt}{\sqrt{2\pi}\sigma_\tau^3} \exp\left(-\frac{t^2}{2\sigma_\tau^2}\right) \quad (2)$$

* Supported by the National Science Foundation of China 11575181, 11375178

And by the Fundamental Research Funds for the Central Universities WK2310000046, WK2310000056

[#] zhouzr@ustc.edu.cn

The peak voltage of the sum signal:

$$V_{\Sigma-peak} = K_P \frac{eN}{\sigma_\tau^2} \propto \frac{Q}{\sigma_\tau^2} \quad (3)$$

$V_{\Sigma-peak}$ is related with bunch electricity quantity Q and bunch length σ_τ . σ_τ changes when bunch current changing in a storage ring. And σ_τ of each bunch is considered as the same value when even filling pattern (HLS-II operates with even filling pattern, each bunch has approximately the same current). When the total beam current of storage ring is known, the BxB beam current could be calibrated by total beam current. The DCCT (DC Current Transformer) measures the total beam current by magnetic field excitation method, not affected by bunch length, and it could be used to calibrate the BxB beam current.

To fulfil peak voltage sampling, the ADC clock need to be phase shifted to find the peak. As shown in figure 1, ADC clock is provided by FPGA, and its signal processing is shown as figure 2.

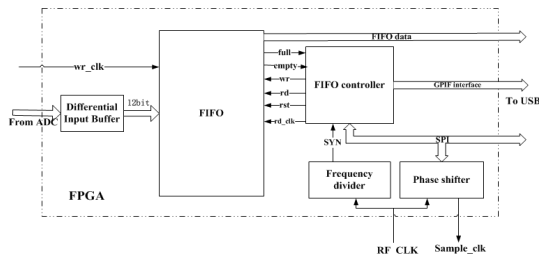


Figure 2: Clock signal processing inside FPGA.

The FPGA's clock is from RF signal of storage ring, 204.03MHz, and it is put into frequency divider and phase shifter inside FPGA. The frequency divider divides the RF signal by 45 (harmonic of storage ring), to get the synchronization signal SYN, 4.534MHz, to synchronize the bunch number inside the FPGA for further data process. The phase shifter uses the DCM (Digital Clock Manager) of FPGA to implement delay lines inside the clock lines with step of ten-picosecond, and the number of delay line could be 0-1023.

Calibration with DCCT

BxB beam current is calibrated by DCCT value, and its relation is described as:

$$I_i = KA_i, i = 1,2,3,\dots,N \quad (4)$$

Where A_i is the peak voltage of sum signal of BPM of each bunch, sampled by ADC, and I_i is actual BxB beam current. And the calibration coefficient K can be calculated as [3].

$$K = \frac{I_{dcct}}{\sum_{i=1}^N A_i} \quad (5)$$

Where I_{dcct} is total beam current of the storage ring from DCCT system, obtained by EPICS access via CA Lab, and processed by a LabVIEW program.

BxB Beam Current Monitoring and BxB Longitudinal Tune Measurement

The depth of FIFO of FPGA is 65536, determining the size of data for single sampling. 45 groups of data are built to get turn-by-turn data for each bunch, and the size of each group is 1456 (65536/45). BxB beam current was calculated by equation (4), calibrated with DCCT, and A_i is the mean value of each group data.

The FIFO data in FPGA could be used to detect the BxB longitudinal tune, as described in figure 3. Solid line is real position of bunch BPM signal, and dashed line is ideal bunch position. 'b' and 'd' are both trough for ADC sampling data, and the ADC data experience two period of oscillation when longitudinal oscillation occurs once. The longitudinal tune could be measured via FIFO data, half of the spectrum of ADC data.

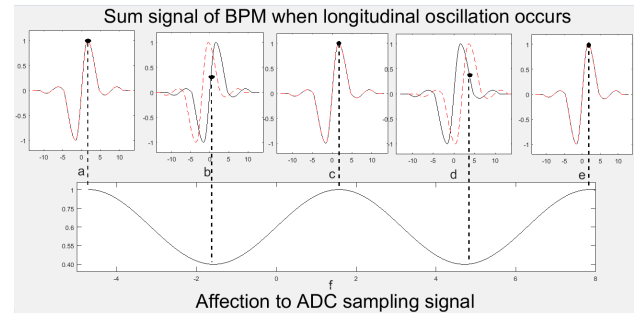


Figure 3: Affection to ADC sampling signal by longitudinal oscillation.

COMMISSIONING RESULTS

The BxB and selected bunch information could be read from the LabVIEW GUI. Figure 4 shows the BxB beam current measurement result with the filling pattern of one single bunch and a bunch train of 34 bunches. The specific bunch current is presented on GUI via inputting the bunch number, and the DCCT value is also presented on GUI.

Copyright © 2016 CC-BY-3.0 and by the respective authors

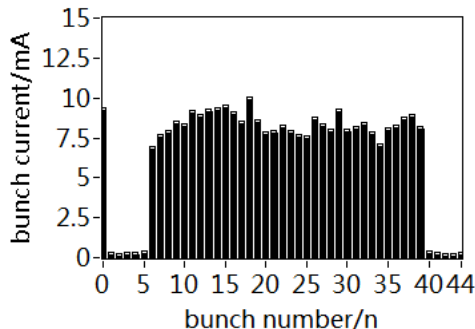


Figure 4: BxB beam current measurement.

The BxB longitudinal tune could be measured via calculating the spectrum of ADC data of each bunch. By turning off the longitudinal BxB feedback system, there is a peak around 50KHz on the spectrum of selected bunch #9, shown as figure 5, which implies the longitudinal tune of bunch 9 is 25KHz.

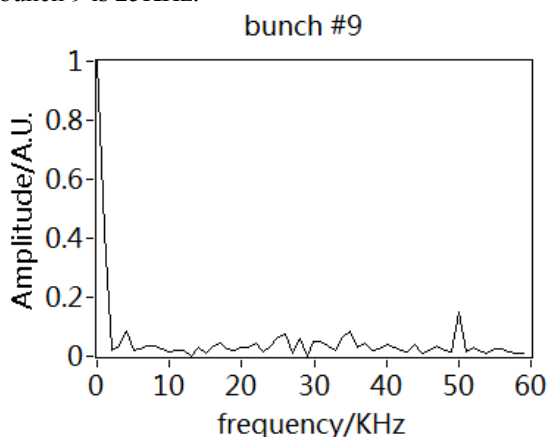
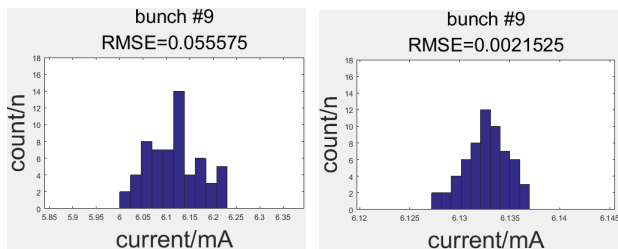


Figure 5: spectrum of selected bunch #9.

The RMSE of the beam current of bunch 9 is calculated when the longitudinal feedback off and on, which is shown as figure 6. When feedback off, the RMSE is about 0.056mA, and the RMSE is about 0.002mA when feedback on.



(a) Feedback off (b) feedback on

Figure 6: The RMSE of bunch #9 affected by longitudinal BxB feedback system.

The peak voltage detection method of bunch current measurement is sensitive to the longitudinal oscillation. And the longitudinal oscillation worsen the precision of the measurement, which should be suppressed.

Figure 7 records the summation of ADC data of the BPM peak voltage of every bunch vs the DCCT value, when the beam current of the storage ring decays from 310mA to 180mA. The dashed line on the picture is the ADC data, and the solid line is the fitting line, and the slope of the fitting line is the calibration coefficient K of equation (5).

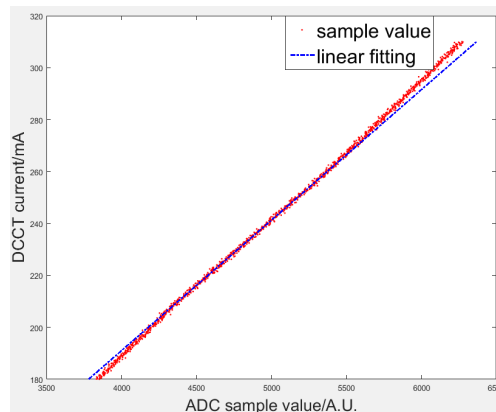


Figure 7: DCCT current with ADC peak voltage data.

The distribution of ADC data on the figure 7 shows the bunch lengthening effect: When higher beam current, the bunch is lengthened, and its peak voltage is lowered. The ADC data is above the fitting line when higher beam current, and below the fitting line when lower beam current.

SUMMARY

An FPGA-based bunch-by-bunch beam current monitor system is developed at HLS-II. The BxB beam current and BxB longitudinal tune could be measured by peak voltage detect of the sum signal of BPM. More bunch-by-bunch beam diagnostics could be done by this system in future, like BxB beam life etc. Peak voltage sampling method is greatly affected by longitudinal oscillation, which worsen the measurement results of the system, should be noticed and suppressed.

ACKNOWLEDGMENTS

The authors would like to present their thanks to the operation staff of HLS-II for their support during machine study. And also thank to Prof Jingyi Li for the discussing and supporting during this study.

REFERENCES

- [1] Lin W, Weimin L, Guangyao F, et al. The upgrade project of Hefei light source (HLS). Proceedings of IPAC 2010, Kyoto Japan. 2010: 2588-2590.
- [2] Yang Y L, Ma T J, Sun B G, et al. HLS bunch current measurement system[J]. Science China Physics, Mechanics and Astronomy, 2011, 54(2): 309-312.
- [3] Sun B G. Beam Diagnostics in Accelerator [M]. University of science and technology of China (2008).