THE FAST INTERLOCK CONTROLLER FOR HIGH POWER PULSE MODULATOR AT PAL-XFEL

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Abstract

The modulator control system for PAL-XFEL consists of a PLC unit (Programmable Logic Controller) and FPSCM (Fast Pulse Signal Conditioning Module). There are two kinds of interlock, which are dynamic and static interlocks categorized as analogue monitor and control signals, digital monitor and control signals. In case of dynamic interlocks, the internal interface of the PLC unit had to be modified due to operating within 10 ms time response from the interlock event. The fast pulse signal conditioning module is adopted for preconditioning the fast pulse and DC signals that inherently have high noise levels generated from a beam voltage, a beam current and EOLC current. Those EM (Electro-Magnetic) noises are generated by thyratron switching. The amplitude of the thyratron noise is large which causes the problem at the control devices, frequently. In this paper, the test results of the interlock control system will be described.

INTRODUCTION

Control system of modern accelerators such as KEKB and J-PARC at KEK adopt many PLCs. They use many types of Programmable Logic Controller (PLC) mainly for an interlock system [1]. PAL-XFEL modulator system also needs the interlock system for handling several interlock sources to prevent serious damage of our equipment. We have two kinds of interlock categories from digital monitors. One is static, and the other is dynamic. In case of dynamic faults, they need the fast response time to halt a modulator operation because it must be stopped before next triggering to the modulator. In order to decrease a response time at dynamic interlocks, we got rid of a digital output relay from a PLC relay box, and set up an optic converter board inside the PLC.

PAL-XFEL modulator controller consists of a fast pulse signal conditioning module and a PLC. A high level switching noise from thyratron switching and a capacitor charging power supply (CCPS) as a dc source of the modulator can lead to equipment malfunction. The fast pulse signal conditioning module was used for preconditioning a fast noisy pulse and dc signal which inherently have high noise levels such as a beam voltage, a beam current and EOLC current

FAST PULSE SIGNAL CONDITIONING MODULE

The FPSCM deals with very noisy and fast varying pulse and DC analog signals. Noisy and short pulse signals generated from the modulator system are beam-V, beam-I, and EOLC-I. These signals are categorized as dynamic interlock signals. The controller must be able to manage real time data. In addition, due to a high noise level within the signals, they should be preconditioned before bringing them to little electrical noise in the control system to avoid its malfunction.

Configuration of the FPSCM

The block diagram of FPSCM is shown in Fig. 1. The multi-sampled analogue data are converted to digital with the ADC in Fig. 1. The micro-processor unit (MCU) is then collect the digital data to calculate an average value. The value is then converted to an analogue signal before providing it to an analogue input module, F3AD08-6R, in a modulator PLC. Noise signals are filtered during the process of multi-point sampling and averaging. All processed signals are isolated with isolation amplifiers before providing to the PLC. ADC is employed to convert analogue to digital signal. The ADC has 10-bit resolution and around 6 μs signal conversion time. DAC is employed to convert digital to analogue signal. The DAC has 12-bit resolution and 4 μs signal conversion time at positive full-scale change. Therefore, total minimum data processing time of sampling is approximately 11 μs. This time is short enough to process the modulator signals at 60 Hz repetition rate.

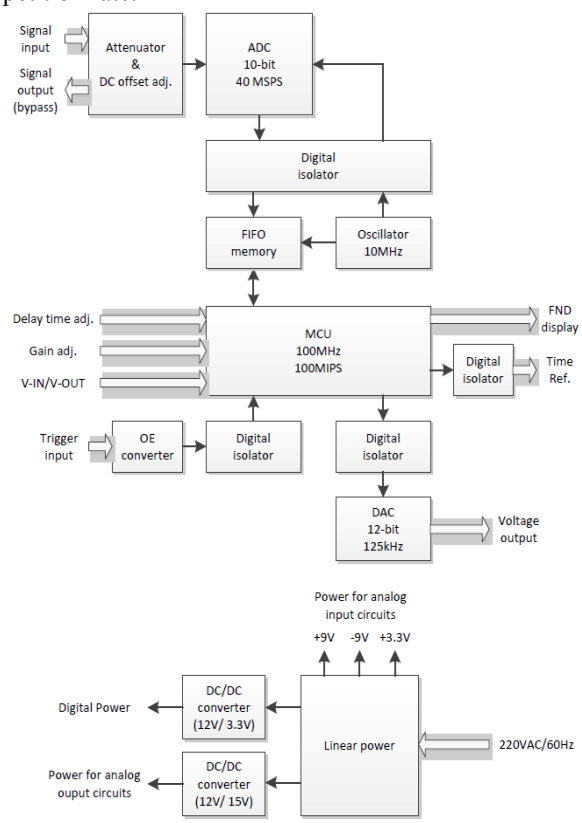

Figure 1: Block diagrams of FPSCM.

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Figure 2 shows a photo of a FPSCM. The front panel for FPSCM made up of four independent channels, which are beam-V, beam-I, EOLC-I, and a spare one.

Figure 2: A picture of a FPSCM

The output signals of FPSCM are 0 ~ +10 V dc signal with very low electrical noise levels. Table 1 shows analogue input and analogue dc output. These output signals are connected with the input module of the modulator PLC via a double shield BNC with ferrite cores.

Table 1: FPSCM Input and Output Signals

Module	Analog Input (Pulse Signal)	Analog Output (DC)
Beam-V	0 ~ - 40 V	0 ~ + 10 V
Beam-I	0 ~ - 40 V	0 ~ + 10 V
EOLC-I	0 ~ + 40 V	0 ~ + 10 V
Spare	-	-

Input signal levels from capacitor voltage divider (CVD) and current transformer (CT) inside a modulator and a pulse tank are adjusted at a voltage divider. The input signals to an input port of the FPSCM as shown Fig. 3 are pulse voltage, which are -40 V at maximum. At the pulse signals such as beam-V and beam-I, the sampling time for 3 μs will be starting to being based on falling time from Time Ref. trigger. Thirty points at an interval of 0.1 μs can be picked up during sampling for 3 μs from beam-V and beam-I. The sampling time must be synchronized with an external trigger, which also triggers a thyratron of a modulator. By receiving the synchronized trigger signal from DG645 installed in a modulator control rack, the module generates sampling start and end time. The sampling time can be adjusted to avoid high noise signal areas where it is a period of a thyratron switching during a modulator operation.

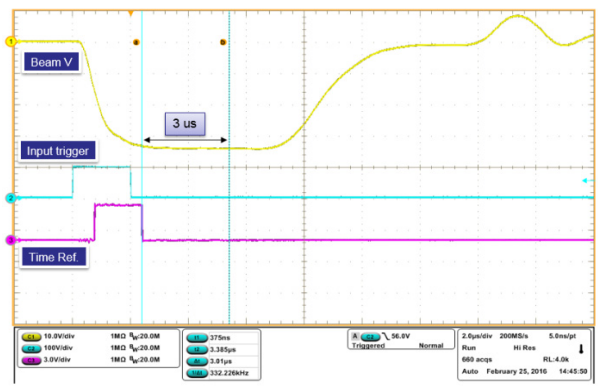

Figure 3: A waveform of beam-V

An end of line clipper (EOLC) circuit is adapted to prevent reverse arcing and over voltage on the PFN capacitors and a thyratron tube during the next charging cycle. The reverse reflected power from a klystron load or other malfunctioning points is absorbed in the EOLC circuit. Fig. 4 is a waveform of EOLC-I. At the pulse signals such as EOLC-I, the sampling time for 10 μs will be starting to being based on falling time from Time Ref. trigger. Only three points at a peak of interval at 0.1 μs during sampling period can be picked up from EOLC-I to process to dc voltage in order to recognize PLC AD modules.

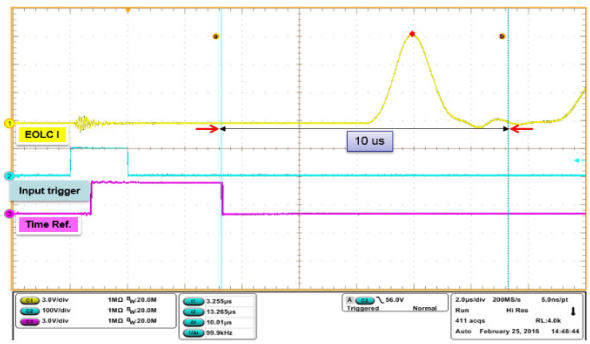

Figure 4: A waveform of EOLC-I

PLC

Signal Type and Operation Sequence of PLC

Figure 5 shows signal types of a modulator interlock. The signals can be categorized as the analogue monitor and signals, the digital monitor and signals, and digital controls. Total number of signals is 103 for one modulator system. SP66-45 CPU and F3RP61-2L, embedded EPICS system, were selected from Yokogawa Electric Co.,Ltd. for the PLC.

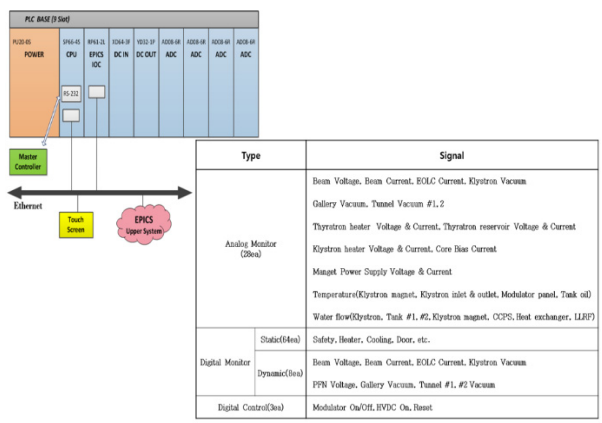

Figure 5: Signal types of a modulator interlock

Figure 6 shows operation sequence of the modulator system. It initially checks interlock status before turning on HVDC when the PLC receives “on” command. If all operating conditions are cleared out, it sets HVDC reference to run the modulator. During running it continuously monitors all static, dynamic, and trigger interlocks. When

detects interlock signals, a typical action is to stop ccps output to block dc source voltage to the modulator. If the system has serious malfunction from static or dynamic faults, the PLC completely turns off the modulator and waits for operators to check out and reset.

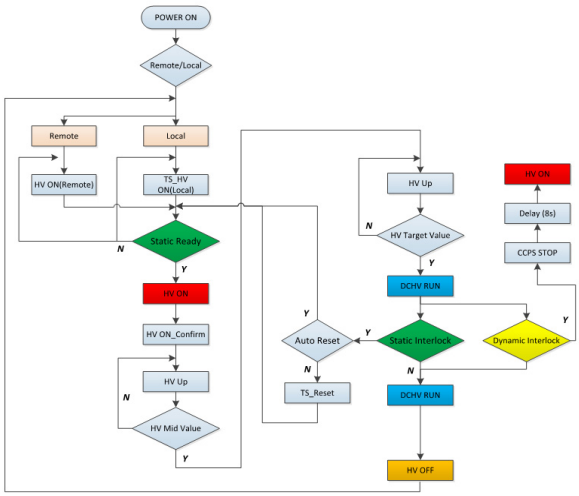

Figure 6: Operation sequence of the modulator

Changing Dynamic Interlock Position in PLC

There are two kinds of digital monitors in the PLC. One is statics (64). The other is dynamic (8). In case of the static interlocks, even though the interlock response time is relatively slow within 10 msec, it is acceptable enough due to contact signals immediately halting the modulator operation at 60 Hz. Dynamic interlocks such as klystron vacuum, gallery vacuum, tunnel vacuum, beam-V, beam-I, and EOLC-I need requirement of dealing with the interlock in very quickly within 2 msec in order to protect the modulator system from its damage. Fig. 7 is drawing of interlock delay when beam-V interlock occurred. Before modifying a relay in an analogue input module to an optic device, an interlock delay time at beam-V was about 15.4 ms. However, after modifying AD conversion cycle and change a relay in an analogue input module to a photo coupler device, an interlock delay time at beam-V was about 1.7 ms. It is acceptable to an interlock response time for beam-V, beam-I, and EOLC-I due to halting next trigger.

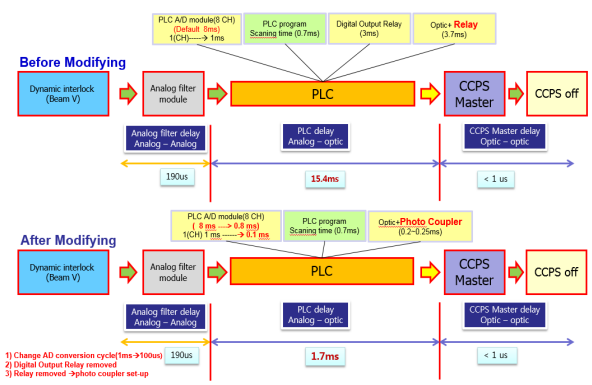

Figure 7: Drawing of interlock delay at beam-V

Figure 8 shows the inside of the PLC. An optical board was installed in order to replace a relay in an analogue input module. All of the changed relay to optical were eight, which were dynamic interlocks such as beam-V, beam-I, EOLC-I, klystron Vac., pfn-V, gallery Vac., and tunnel Vac.

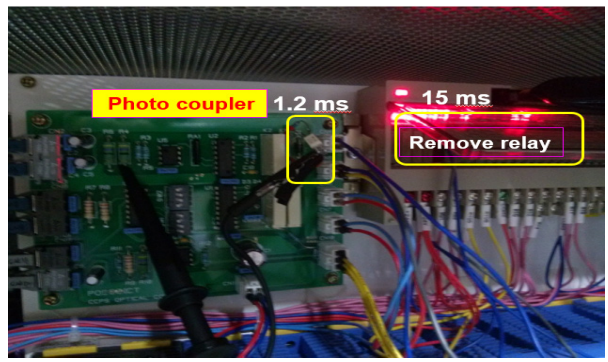

Figure 8: The inside of the PLC

Figure 9 is waveform to measure an interlock response time between beam-V fault and interlock point on the optic converter board.

Figure 9: Measurement of an interlock response time

SUMMARY

There are many noisy signals in a pulse modulator system. In other to receive a clean signal from beam-V, beam-I, and EOLC-I, FPSCM was developed and has been installed on the modulator control system. Owing to FPSCM, the value of beam-V, beam-I, and EOLC-I can be displayed on the screen of a PLC exactly, and also their interlock speed can be working quickly on the PLC.

In case of dynamic interlocks, it is very important to decrease the interlock response time to shut down before 2 msec to prevent CCPS output power from charging to PFN in the pulse modulator. As shown Fig. 7, after modifying AD conversion cycle and change a relay in an analogue input module to a photo coupler device, the interlock delay time was acceptable.

REFERENCES

[1] K. Furukawa et al., "DEVELOPMENT OF EMBEDDED EPICCE ON F3RP61-2L," in the proceedings of PCaPAC08, WEX03.

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