A DIGTAL REGULATION CONTROLLER PROTOTYPE FOR THE TPS BOOSTER POWER SUPPLIES

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Abstract

In the newly built TPS (Taiwan Photon Source), the AC power supplies of the Booster ring are required to operate in DC and AC mode with accuracy. Especially in AC mode, during the booster ramping process, the current ramping profiles of the Quadruple Magnets have to track that of the Dipole AC power supply with precise phase and amplitude to maximize the beam energy boost efficiency. At the present time, analog controllers are used for all the booster supplies and the tracking waveforms are generated externally in an EPICS control unit, converted to analog signals with precision Digital-to-Analog Converters (DACs) and then distributed to all the booster power supplies with differential signal pairs. In this paper, a new digital regulation architecture is proposed. In the new architecture, the current ramping profile data is stored digitally in each power supply and then output to each power supply with a synchronous trigger signal and the power supply regulation loop is also implemented digitally in hope to eliminate the signal integrity problem inherent in analog signals so that the beam energy boost up could be more reliable and efficient. The new proposed architecture has been implemented and tested successfully and will be applied to the booster power supplies to test its performance in the near future.

INTRODUCTION

The booster ring had been successfully commissioned and the electron beam was accelerated efficiently from 150MeV to 3 GeV with 3Hz repetition rate on December 16 2014. At the end of 2015, the TPS stored beam current had been pushed to 521mA, which is beyond the designed 500mA goal.

The control infrastructure of the TPS booster ring power supplies is illustrated in Figure 1[1].

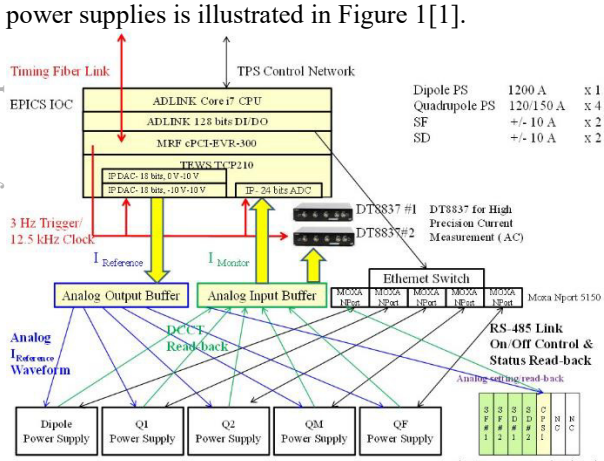

Figure 1: The control of TPS booster ring power supplies.

As shown in Figure 1, an EPICS control unit is responsible for controlling and monitoring the booster ramping power supplies in a synchronous manner. Digital ramping waveform data profile are preloaded to the unit through Ethernet, converted to analog differential signals by 20 bits DACs and then output to all the booster ramping power supplies synchronously. High resolution 24 bits Analog-to-Digital Converter (ADCs) DT8837 are used to provide more high precision current monitoring.

The booster ring energy ramping efficiency mainly depends on the independent tracking error of the input reference and actual output current waveform of dipole and quadruple power supplies and the relative tracking error of the input and output of the quadruple ones respective to that of the dipole power supply. However, due to 1)the different booster dipole and quadruple magnet loading, 2)the limited bandwidths of the various types of booster dipole and quadruple power supplies and 3)the analog control scheme vulnerable to electrical noise, it is not an easy task to keep the tracking error well below the desired 0.2% NRE (Normalized Relative Error respective to reference) at the injection point. Efforts have been made to minimize the NRE with waveform compensation strategies and enhance the noise immunity with analog differential transceiver, by which the NRE is barely supressed below the desired 0.2% value. In this paper, a full digital regulation architecture is proposed in order to overcome the current tracking error issue and push the NRE as low as possible.

DIGITAL CONTROL SCHEME

The proposed full digital regulation architecture has been implemented and first applied to control a TPS corrector power supply and corrector magnet load to test the performance as requested.

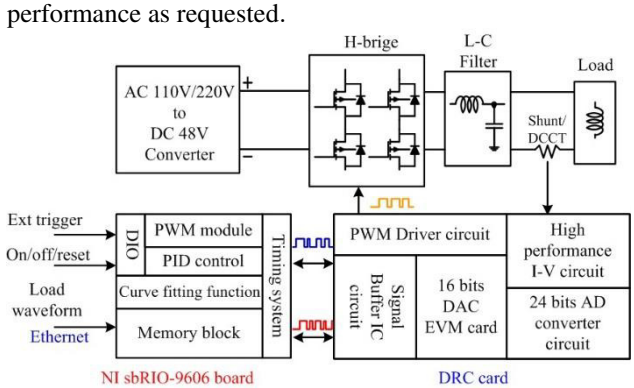

Figure 2: Digital Regulation Control Architecture.

Figure 2 shows the digital regulation architecture, which is composed of four building blocks : an NI embedded device with FPGA and digital IO card, a DRC card (digital

regulation control card), a TPS corrector power converter and a TPS corrector magnet load. The major functionality of each block is to be explained in the following section.

TPS Corrector Power Converter

This bipolar power supply is specially designed for TPS corrector magnets. The converter can delivers +/- 10 Amperes up to 48V. Figure 3 shows the picture of the corrector converter, which is buck converter employing full bridge MOSFETs as switches and high precision DCCT as feedback element. The current output long term stability within 16 hours is well below 10 ppm [2-4].

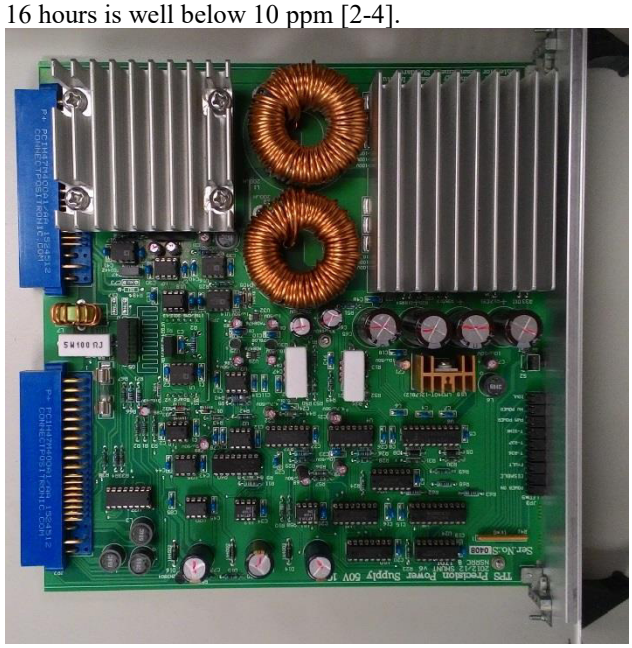

Figure 3: TPS corrector power module.

NI Embedded Board with FPGA

This bock is implemented with NI sbRIO-9606 single board computer equipped with Xilinx Spartan 6 FPGA and DIO (digital Input Output) extension card, which performs the major tasks as follows:

- Communicating with external EPICS node to accept synchronous trigger, current ramping profile, waveform compensation and PI control parameters.
- Digital PI control controller.
- Current ramping profile compensator.

The digital closed-loop control block diagram is depicted in Figure 4. The red dash block is implemented here in the FPGA using VHDL (very high descriptive language) code. The PI control gains can be changed on the fly from remote control panel.

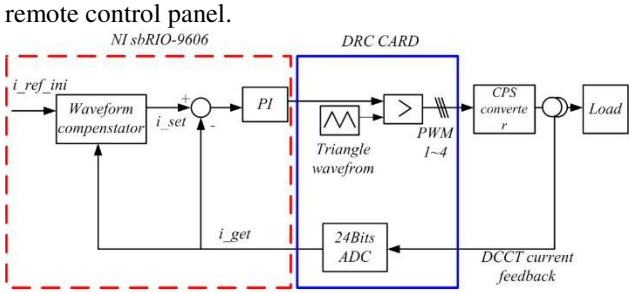

Figure 4: Digital closed-loop control block diagram.

The current ramping waveform compensator block is illustrated in Figure 5. This functionality of this bock is to minimize the tracking error between the reference current command and the actual current output waveform. The algorithm used is Proportional and Time Shift Compensation [5].

$$i\_set_{(n+1)}(t) = i\_set_{(n)}(t) + i\_ref(t-\tau) - i\_get_{(n)}(t-\tau)$$

First, the time shift delay between the current command and output is measured and then input to the equation for waveform compensation. Second, reference waveform is played for several iterations to compensate the error difference.

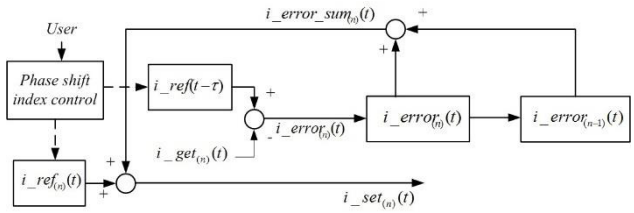

Figure 5: Waveform compensator block.

Digital Regulation Control Card

In this control card, two major functions are implemented. They are 1) Convert the current command after the PI controller to PWM switching signals to control the on-off switches of the full bridge MOSFETs, 2) Translate the incoming current feedback from the DCCT to voltage signal and then digitize it using 24 Bits ADC (analog to digital converter) for digital control loop feedback and 3) Optional 16 Bits DAC channels are also embedded for real-time display of both reference and current output waveform for easy comparison purpose through external digital oscilloscope [6]. The photo of the control card is shown in Figure 6.

Figure 6: Digital regulation control card.

EXPERIMENTAL RESULTS

Figure 7 shows the virtual software interface for the overall proposed digital control scheme. The reference waveform generation, PI controller gains, waveform compensation parameters *etc* are all accessible through the interface, which is realized by NI Labview.

It is shown in Figure 8 the waveforms of the reference input and current feedback and the NRE error when the tracking error compensation function is disabled. It can be

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observed that there is a phase lag between these two waveforms due to the controller and the magnet loads.

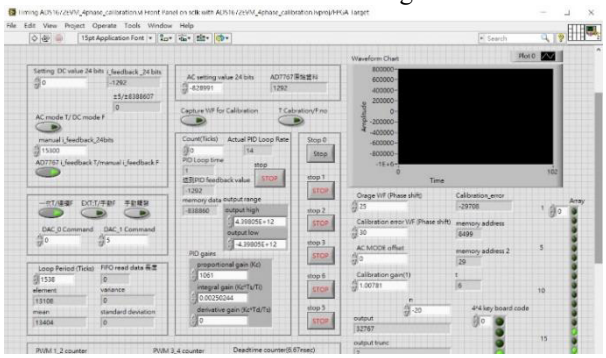

Figure 7: Virtual software control interface.

The control goal is to make this time shift and tracking error as small as possible if the proposed scheme is to be used to replace the present analog control scheme of the TPS booster ramping power supplies. Figure 9 illustrates the waveforms of the reference input and current feedback and the NRE error after three iterations when the compensation function is enabled. It is shown with compensation function enabled, the NRE is largely reduced and it takes only 2~3 iterations for the NRE to fall below 0.1% at the 13.5ms injection point during the 333ms time period of the 3 Hz ramping frequency for TPS booster ring ramping.

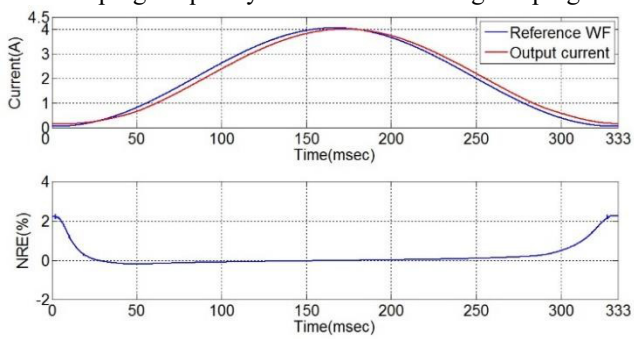

Figure 8: Reference and output waveform and NRE when waveform compensation is off

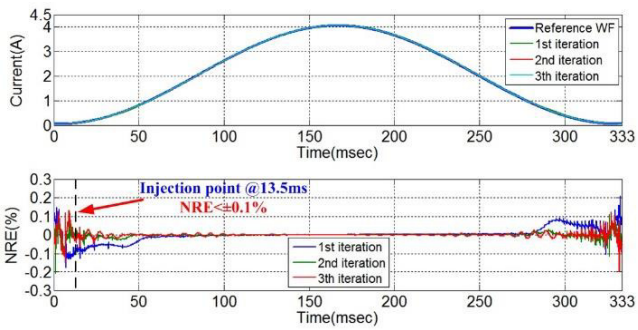

Figure 9: Reference and output waveform and NRE when waveform compensation is on.

CONCLUSION

A new digital regulation architecture for TPS booster ramping power supplies is presented. This preliminary prototype is first applied to the TPS corrector power converter to evaluate whether the specified requirements are met. It has been proved in the experiments that this digital architecture is capable of auto calibrating the internal current command so that the power converter's current output waveform will converge to that of the incoming 3 Hz reference with NRE error well below 0.2% during the 3 Hz ramping cycle. After the successful tests, this proposed architecture will be applied to the booster ramping power supplies in the near future, hoping to eliminate the signal integrity problem inherent in analog signals so that the beam energy boost up could be more reliable and efficient.

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