DESIGN AND IMPLEMENTATION OF EMBEDDED APPLICATIONS WITH EPICS SUPPORT FOR ACCELERATOR CONTROLS

Y. S. Cheng, Demi Lee, C. Y. Liao, C. H. Huang, K. H. Hu, K. T. Hsu
National Synchrotron Radiation Research Center, Hsinchu 30076, Taiwan

Abstract

Low-cost card-size SBCs (single-board computer) are with small footprint, powerful in CPU performance and rich interfaces solution to widely adopted for educational purposes and also suitable for small scale embedded applications. The card-size SBCs have been applied for several applications with EPICS support at the TPS control system environment as auxiliary supports which are not suitable to use standard platform in existed control system due to economics, simplicity, specialty view points. The more efforts of several implemented applications are summarized in this paper.

INTRODUCTION

Using a circuit board to implement functions as a computer is called SBC (single-board computer) [1]. Its applications cover in telecommunications, industrial control, blade and high density servers, and lately laptops and mini-PCs, etc. Duo to the latest generation SoC technology, putting all major functionality into an integrated chip, educational used credit-card size SBC [2] likes the Raspberry Pi (RPi) and Banana Pi (BPi) are highly successful products. The BPi is the latest product of such category with powerful CPU, low power consumption SBC indeed, and the area of circuit board is only as credit card size.

The BPi which design idea is similar to the RPi-style SBC, and it is a fork of the RPi project using different components while maintain compatibility as much as possible. Moreover the BPi is added the functions of SATA interface, infrared transmission, microphone, USB-OTG ports, power button, reset button, etc. Then the BPi has 40-pin GPIO which is compatible with the RPi. The A20/A31S/A83T SoC as CPU/GPU, DDR3 memory and Gigabit Ethernet connection are applied on the BPi. The hardware specification of BPi is shown as Table 1 [3]. Linux-based OS can be worked well on the BPi.

Table 1: Hardware specification of the Banana Pi

	Banana Pi M1+/M2/M3
CPU	A20 ARM Coretx-A7 1GHz Dual-core A31S ARM Coretx-A7 1GHz Quad-core A83T ARM Cortex-A7 1.8GHz Octa-core
Memory	1GB DDR3 RAM / 2GB LPDDR3 RAM
Network	1Gbps Ethernet RJ45, Wi-Fi
Storage	SD card slot (up to 64GB), Extensible with SATA interface
I/O	GPIO, UART, I2C bus, SPI bus with two chip selects, CAN bus, ADC, PWM, +3.3V, +5V, GND
OS	Debian, Bananian, Ubuntu, Android ...

The EPICS (Experimental Physics and Industrial Control System) [4] is a set of open source software tools, libraries and applications developed collaboratively and used to create distributed soft real-time control systems for scientific instruments such as particle accelerators. Many facilities have good practical experiences for the EPICS and adopt it as accelerator control systems. Many resources and supports are available as well as numerous applications for accelerator have been developed.

The TPS (Taiwan Photon Source) control system of 3 GeV synchrotron light source is also based on the EPICS framework [5]. The EPICS toolkit provides standard tools for display creation, archiving, alarm handling, etc. The big success of EPICS is based on the definition of a standard IOC (Input Output Controller) structure together with an extensive library of driver software for a wide range of I/O cards. The EPICS framework which has various functionalities is employed to monitor and to control on embedded applications of accelerator system.

BANANA PI AS EPICS IOC

The stability and performance of Banana Pi (BPi) is enough as the EPICS IOCs for specific control applications. The EPICS framework can be built on the Linux-based BPi successfully [6]. At the TPS project, some control functions, such as direct digital synthesizer, frequency divider, alarm announcer, radiation-sensing reader, etc., are implemented by use of the BPi platforms with EPICS support. The efforts of implementation are summarized as followings.

Software Architecture

To implement the BPi as the EPICS IOC for specific control applications, the EPICS base and modules are necessary to be set up on the BPi platform which operation system can be the Debian or Ubuntu Linux. The device driver of SPI (Serial Peripheral Interface) bus is built for communicating with DAC/ADC modules, and the device support interface is also developed as the glue between the EPICS records and device drivers. The EPICS records support with databases are created according to the specific functions. The application module, such as “autosave” function, is installed for logging setting parameters values and recovering last setting parameters values automatically when the IOC is start-up. Based on the EPICS PV (Process Variable) channel access, the archive server is set up to record various parameters variations for long time observation, and the PHP webpage can be developed to show the status information. At the client console side, the operation interfaces are created by used of the EDM, CS-Studio, etc.

to control and monitor via EPICS PV channel access, and the archived data can be retrieved with using a form of graphical representation of the CS-Studio based data browser. The schematic is shown as Fig. 1.

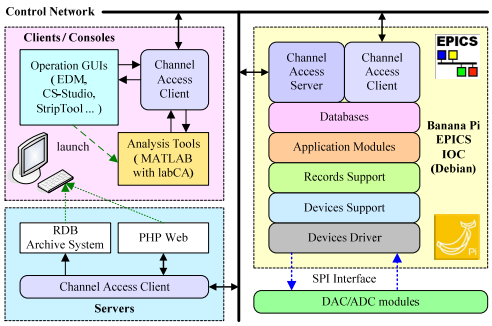

Figure 1: Software architecture of the BPi within EPICS support.

Direct Digital Synthesizer Control

To make possibility of different RF frequency without a similar multiplication factor work for linear accelerator (Linac) and booster synchrotron to optimize machine performance without adjust too many parameters in Linac system, a RF signal generator direct digital synthesizer (DDS) which can synchronize at injection instance have been implemented. Functional block diagram of the prototype is shown in Fig. 2. The BPi EPICS IOC is used to control the DDS to achieve goal. Synchronization is achieved to reset the phase of the DDS just before booster synchrotron injection to ensure constant phase relationship between RF system of Linac and booster synchrotron. Fig. 3 shows the prototype DDS signal generator. Fig. 4 shows the RMS jitter of implemented DDS signal output is 0.3 picosecond approximately.

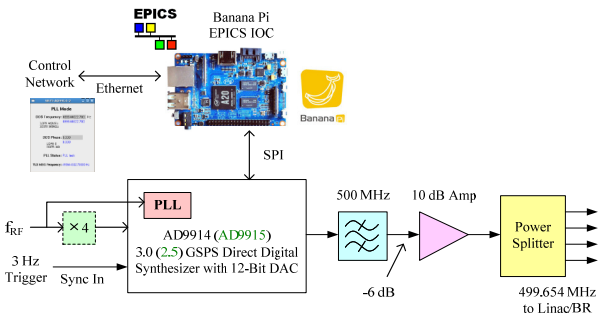

Figure 2: Block diagram of the DDS control.

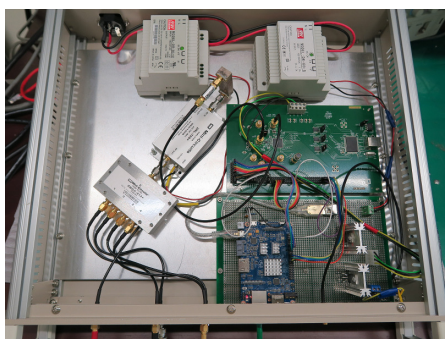

Figure 3: Photo of the DDS signal generator.

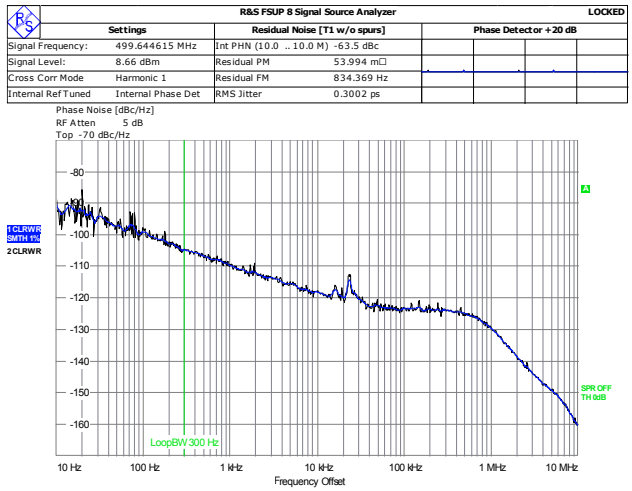

Figure 4: Measurement of RMS jitter for the DDS signal generator.

Programmable Frequency Divider

Machine clock of the accelerator system generated discrete fast logic chip (ECL/PECL) or combined of fast logic and field programmable logic array (FPGA) usually. Typical jitter is in a few picoseconds order. The programmable clock generator has been implemented by using the AD9508 clock and delay generator to generate clock with 100 femtosecond jitter for some applications (laser clock, filling pattern measurement timing, etc.). The system schematic is shown as shown in Fig. 5. The chip divider and delay parameters can be controlled by use of the BPi EPIC IOC via SPI interface. The implementation is shown as in Fig. 6.

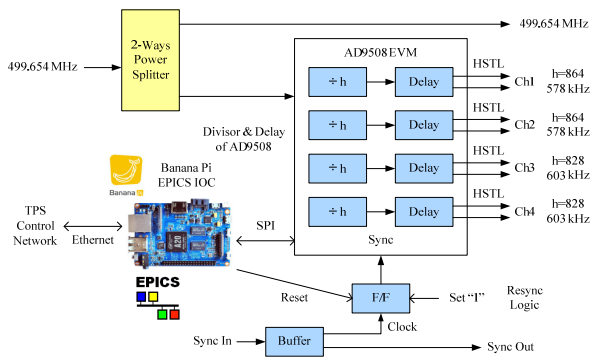

Figure 5: Block diagram of the programmable clock generator.

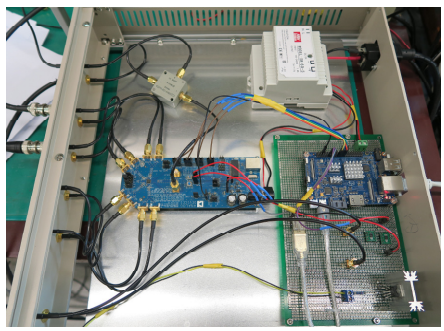

Figure 6: Photo of the frequency divider unit.

ISBN 978-3-95450-147-2

Alarm Announcer

During the TPS commissioning and operation phases, the abnormal status may occur from one of sub-systems, and operators need to find out which sub-system problem happened from machine interlock interface. Due to many interlock signals need to be noticed, the sum signals of each interlock signals are necessary. According to the sum signals, the specific alarm message to be trigged and shown, and the BPi is used as the EPICS IOC to receive the request and send alarm announcement sound to loud speaker for noticing. The system schematic is shown as Fig. 7, and the implementation is shown as in Fig. 8.

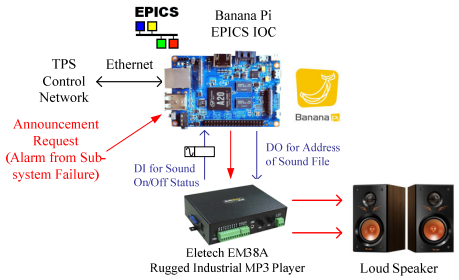

Figure 7: Block diagram of alarm announcer.

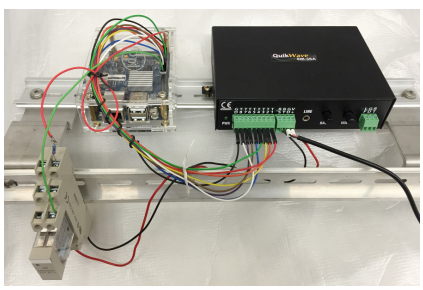

Figure 8: Photo of the alarm announcer with BPi EPICS IOC.

RadFET Reader

To investigate the beam loss and its distribution during commissioning and operation phases of TPS and TLS (Taiwan Light Source), a sixteen-channel readout box was initially designed and implemented to read the threshold voltage of the RadFETs (radiation-sensing field-effect transistor) which were installed at accelerator tunnel [7]. The initial version design was that the reader plays a role of remote I/O for the EPICS IOC and the IOC collects voltage from readers distributed at the accelerator to deduce the integrated dose and dose rate.

The next version design is that the EPICS IOC will be embedded into the RadFET reader box. The BPi will be also adopted as the EPICS IOC for collecting the threshold voltage of the sixteen-channel RadFETs. The data transmission time between the IOC and SPI bus with ADC modules will be improved.

The EPICS IOC performs data acquisition, calculation, and publishes the specific EPICS PVs of dosage. Dosage rate is calculated by the EPICS record processing. All of the threshold voltage values based on EPICS PVs channel access can be recorded into the archive server for further off-line data processing. The MATLAB toolkit can be also used to analyze the RadFET threshold voltage archived data which retrieved from the RDB archive system directly. The control system also provides on-line display for virtualization usage. The system schematic of RadFET reader is shown as Fig. 9. The test prototype of RadFET reader with the BPi EPICS IOC is shown as Fig. 10.

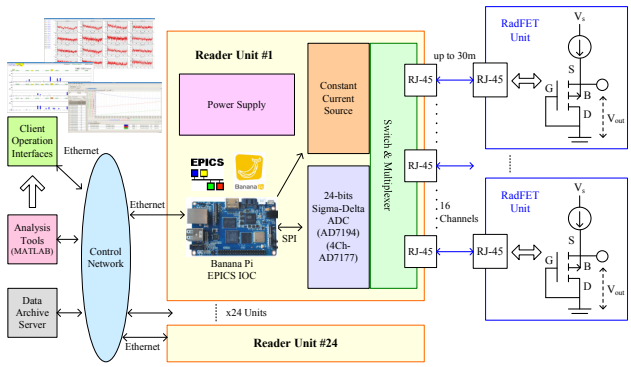

Figure 9: Block diagram of the RadFET readers system.

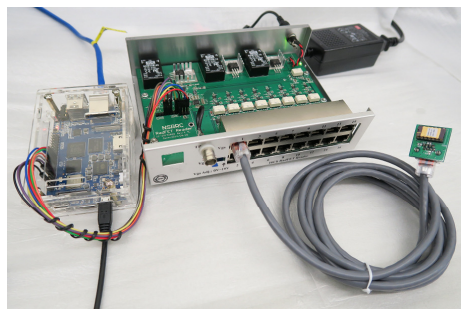

Figure 10: Photo of the prototype 16 channels RadFET reader with BPi EPICS IOC.

SUMMARY

Low cost credit-card size SBC is widely adopted for educational purpose and also suitable for small scale embedded applications. The BPi is chosen for several applications at the TPS control environment as auxiliary supports which are not suitable to use standard platform in existed control system due to economics, simplicity, speciality view points. More applications will be explored and implemented in near future.

REFERENCES

[1] Single-board computer website: https://en.wikipedia.org/wiki/Single-board_computer
[2] Educational single board computer website: http://edutechwiki.unige.ch/en/Educational_single_board_computer
[3] Banana Pi website: http://www.banana-pi.org
[4] EPICS website: http://www.aps.anl.gov/epics/
[5] C. Y. Liao, et al., "Commissioning of the TPS Control System", FRB3O01, Proceedings of ICALEPCS'15, Melbourne, Australia (2015).
[6] EPICS Pi website: http://prjemian.github.io/epicspi/
[7] Demi Lee, et al., "Online RadFET Reader for Beam Loss Monitoring System", MOPTY070, Proceedings of the IPAC'15, Richmond, USA (2015).