RECENT UPGRADES TO THE CERN SPS WIDEBAND INTRA-BUNCH TRANSVERSE FEEDBACK PROCESSOR *

J. E. Dusatko#, J. D. Fox, C. H. Rivetta, O. Turgut,
SLAC National Accelerator Laboratory, Menlo Park, California, USA
W. Höfle, CERN, Geneva, Switzerland

Abstract

In support of the CERN High Luminosity LHC(HL-LHC) upgrade program, a research and development effort has been underway to understand and develop feedback control techniques for mitigating transverse intra-bunch instabilities in the SPS driven by electron cloud and TMCI effects. These effects could be a limiting factor to overall machine performance. A result of this effort has been the development of a very wide band transverse feedback demonstration system. This system has been used for the last several years in machine development studies where we have demonstrated single-bunch stability control of low order intrabunch modes. In continuation of these efforts, recent upgrades have been performed in all stages of the system, including the feedback processor itself. This paper discusses the upgrades specific to it, including the ability to process multiple proton bunches in the SPS; and also highlights future directions in the development effort.

BACKGROUND

One possible limitation of high luminosity operation for the LHC is electron cloud induced instabilities (ECI) and transverse mode coupled bunch instabilities (TMCI) in the SPS [1]. Such instabilities increase with higher beam intensities and can ultimately limit luminosity in the LHC. Several schemes are being pursued [2] to mitigate this effect: changes to the SPS lattice, vacuum chamber coating and active feedback control. The last item has been the focus of our work.

To develop a practical feedback control system, a research and development effort has been undertaken between CERN and SLAC. This effort is multifaceted and involves beam and system dynamics simulation and modelling, technology development and machine measurements. The technology development portion has produced a wide bandwidth 4GSa/s transverse feedback demonstration or "demo" system. Machine development studies involving single bunch beam dynamics have given encouraging results: control of low-order intrabunch (head-tail) mode instabilities has been shown [3]. Building on this, our efforts continue with further refinement of the models and development of advanced control algorithms; both driving improvements to the feedback demonstrator system. The overall demo system has already undergone multiple improvements [4]. Focusing on the feedback processor itself, we outline several upgrades already performed and others in progress or being planned.

*Work supported by the U.S. Department of Energy under contract DE-AC02-76SF00515 and the US LHC Accelerator Research program (LARP) and FP7 HiLumi LHC http://hilumi.lhc.web.cern.ch
#jedu@slac.stanford.edu

SYSTEM OVERVIEW

The transverse feedback demo system is shown in Figure 1. Vertical motion of the beam is sensed by a stripline Beam Position Monitor (BPM) pickup. Pre-processing occurs in the Analog Front End, where an RF hybrid produces the displacement signal, from the four pickup signals. This signal is then amplified, filtered and equalized before being passed to the feedback processor.

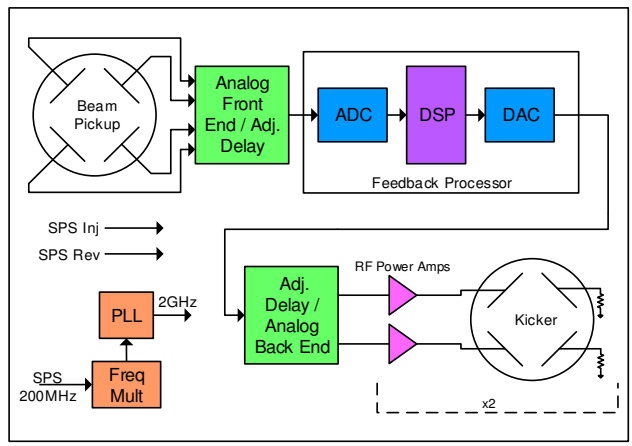

Figure 1: Overall System Block Diagram.

The feedback processor itself is essentially a general-purpose digital signal processing channel. The ADC, sampling at 4GSa/s, takes 16 slices, or samples, across the ~4ns SPS injection bunch. These digitized slices are then passed to the Digital Signal Processor block which computes a correction signal for each slice and then passes them to the DAC, which converts the digital numbers back into analog voltages also at 4GSa/s. Further processing (filtering, equalization, amplification and splitting) is performed by the Analog Back End. The output signal of this block is then sent to two installations of RF power amplifier and kicker structures, which amplify and drive a corrective field onto the beam.

Since the feedback processor can only shift timing in a coarse manner (5ns steps), adjustable delay lines have been added to the front and back ends enabling fine-tuning of the input and output signal timing (in steps of several ps). This "timing-in" process is crucial to measuring and driving the beam properly.

The system sampling clock is generated from the 200MHz SPS RF clock by the frequency multiplier, giving a 2.0GHz clock. Both edges of this clock are used by the output data converter giving an effective giving an effective sampling rate of 4.0GHz. In these initial results, the system has been running at a 3.2GHz clock rate which

ISBN 978-3-95450-147-2

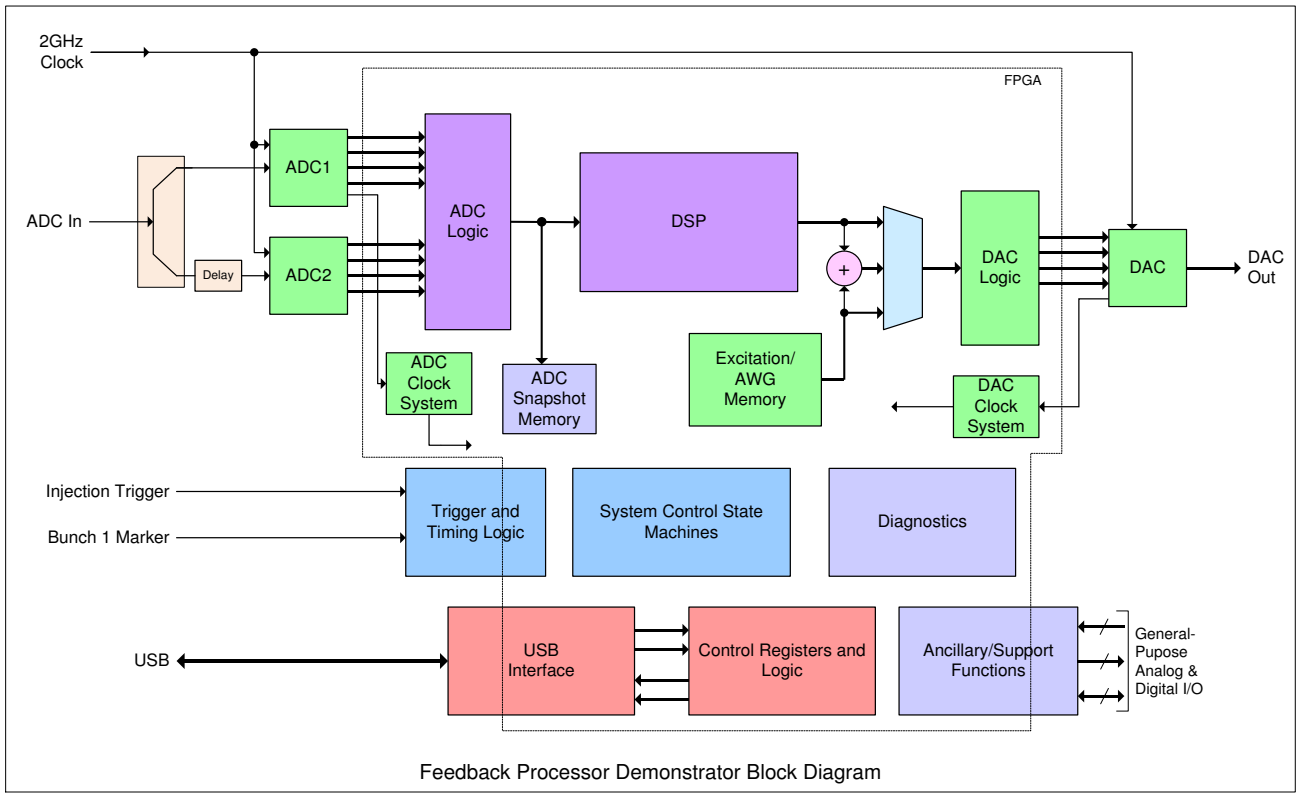

Figure 2: Feedback processor block diagram.

simplifies the synchronization between systems. Future measurements with the wider bandwidth slotline kicker (now in design) will benefit from the full 4GHz sampling rate. The Phase Locked Loop block following the multiplier compares the DAC data clock phase with the SPS RF ensuring phase lock of the output DAC stream. This simplifies timing setup and provides robust resynchronization each startup and timing cycle.

THE FEEDBACK PROCESSOR

The system (in Fig. 2), uses two 2GSa/s 8-bit, Maxim Semi MAX109 ADCs time interleaved to provide the 4GSa/s rate and one Maxim Semi MAX19693 12-bit, 4GSa/s DAC. The FPGA is a Xilinx XC6VHX565T Virtex-6 FPGA. Communication with the host computer is via a USB 2.0 interface. System software is implemented using Visual Basic for system control and offline data processing and analysis is done with Matlab tools that we have developed for this application. A salient feature to note is that the majority of system functions (inside the dotted line) are implemented inside the FPGA. This provides great flexibility in the design.

UPGRADES

Multiple Bunch Processing

For expediency in development, the original design of the processor controlled single bunches, consistent with the study of intra-bunch effects. A practical system however, must be capable of controlling all bunches in an LHC fill. The processor's FPGA design was modified to enable multiple bunch processing by moving to a double-buffered buffered dataflow architecture and adding in a multi-channel FIR filter.

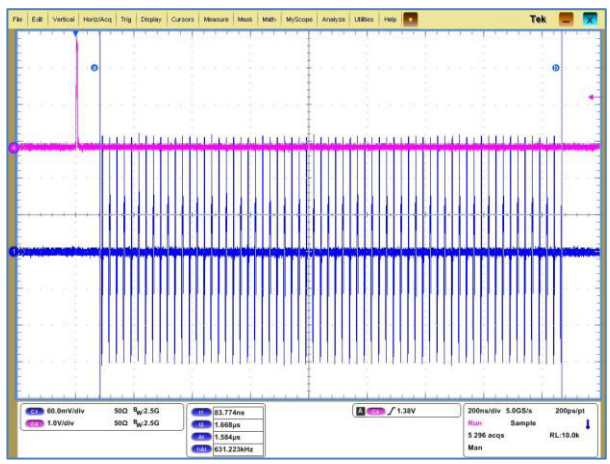

Figure 3: Processing 64 bunches at 25ns separation, each bunch has 16 unique control samples across the 5ns sample window

This enables [1…64] sequential bunches to be controlled. The upper limit is driven by FPGA resources. This feature also enables [1…32] bunch doublets (normally utilized in machine scrubbing operation) to be proceed. The double-buffered FIFO dataflow pipeline simplifies clock domain crossing and makes changing of the core DSP function much simpler (essentially different DSP algorithms can be "plugged

in"). Figure 3 shows an oscilloscope photo of the system processing 64 bunches. The signal is measured at the DAC output, with the ADC receiving stimulus from a frequency synthesizer and the FIR filter simply multiplying by one. The upper trace displays the fiducial trigger.

Feedback + Excitation Combined Mode

It is useful for grow/damp studies to have the ability to excite the beam by driving it with a tailored signal, while simultaneously running feedback. Plus, the ability to have a synchronized arbitrary excitation and simultaneous record of bunch motion is vital for bunch dynamics identification. This was originally accomplished using a separate hardware excitation system whose output was summed with the feedback processor's in the analog domain. The feedback processor has its own excitation subsystem which had essentially ran stand-alone. The processor's FPGA was modified to perform the feedback + excitation sum digitally, eliminating the need for the external excite system and its complex timing setup.

Individual Sample Gain Controls

Another useful tool for grow/damp studies to is the ability to induce oscillations in the beam by shifting the system momentarily to regenerative (positive) feedback. With this function, the gain of each of the 16 FIR n-tap filter channels (gain of each slice filter) is individually adjustable over a range of [+1…-1], allowing flexible modification of intra-bunch feedback control. Two individual sets of the 16 sample gain settings are loadable and switching between them is automatically controlled by counting the number of SPS turns starting from injection.

Output Waveform Preamble/Postamble

Characterization of the RF power amplifiers revealed that in pulsed operation, the amplifier response produces a tail that bleeds into the next bunch (25ns later). This is comparable to intersymbol interference in a communications system. Simulation studies using measured response data from system components suggest that the addition of a preamble, postamble or even a split pre/postamble, can reduce this effect. These added signals essentially act as an upconverter to modulate the low frequency modal information on a higher carrier. The beam then samples this information back down to the low baseband signal. This feature has been added and provides user selection between the different formats described.

System Software

The system software has been updated to support all of the upgraded features. The capability has been added to sense the loaded system FPGA version and enable/disable features based on that version. A Matlab application has been created that allows real-time viewing of snapshot data as it is collected, greatly assisting MD studies.

FUTURE UPGRADES

Work is continuing on further enhancements. These include: 1) Expansion of the ADC snapshot memory to use much deeper external DDR3 memory, removing the single bunch, 65565 turn maximum record length. 2) Implementation of an Ethernet interface to allow fast transfers of the longer snapshot data. 3) Advanced signal processing algorithms (IIR, observer-based control, etc.) and 4) Beam orbit offset rejection based on taking the DC average of beam position over many turns.

PROCESSING AT 8GSA/S

Progressing to the next generation of feedback processing doubles the sampling rate. This opens up multiple possibilities, including reduction of system noise, exploration of different processing configurations (multiple pickups, etc.) and enhanced diagnostic capabilities beyond transverse feedback control.

The first step in development began with a survey of commercial ultrafast ADC and DAC device, and has led to the selection of promising candidates, the purchasing of evaluation hardware and the beginning design of a prototype system. The first step in development will be the evaluation and characterization of the ADC and DAC devices. A follow-on effort will incorporate these elements into a full 8GSa/s flexible second generation processing platform.

ACKNOWLEDGMENTS

We wish to thank Urs Wehrle and Endre Bjorsvik of the CERN BE-RF-FB section their respective work in integrating our system into the SPS and the output signal pre/postamble simulation studies.

REFERENCES

[1] G. Arduini *et.al.*, "Beam Observations With Electron Cloud In The CERN PS & SPS Complex" ECLOUD04 Proceedings, 2004.

[2] J. Coupard e*t.al.*, "LHC Injectors Upgrade Technical Design Report – Volume 1: Protons," CERN Document, 15-December-2014, CERN-ACC-2014-0337.

[3] J. D. Fox *et al.*, "Wideband Vertical Intra-Bunch Feedback at the SPS - Technology Development, Recent Accelerator Measurements and Next Steps", IBIC2015, Melbourne, Australia, WECLA04.

[4] J. Dusatko *et al.*, "Upgrade and Operation of the Demonstration 4 GS/Sec. Intra-Bunch Instability Control System for the SPS", IPAC2015, Richmond, VA, MOPWI037.