DEVELOPMENT OF 200 MHz DIGITAL LLRF SYSTEM FOR THE 1 MeV/n RFQ AT KOMAC*

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Abstract

As a part of the R&D towards the multi-purpose ion irradiation system, 1 MeV/n RFQ will be developed at KOMAC (Korea Multi-purpose Accelerator Complex). This paper presents the latest Low Level RF (LLRF) test results obtained with 200 MHz dummy cavity. The main focus will be on the programmed FPGA (Field Programmable Gate Array) control logics using the PENTEK7156 based system [1]. Details about the firmware upgrades and future works will be described.

INTRODUCTION

The KOMAC multi-purpose ion irradiation system will include 200 MHz RFQ cavity. This RFQ system requires 1 % amplitude error stability. This RF system controlled through a digital LLRF board and the RF signal amplified with the SSA (Solid State Amplifier) as shown in the Fig. 1. The proposed LLRF system is controlled by only digital control board and samples the RF signal using non-IQ sampling technic. In addition, the digital board directly samples the RF signal to detect RF signal and directly generates the RF signal without the analog components. This current work reports on the firmware upgrades and the FPGA logics to meet the LLRF system configuration.

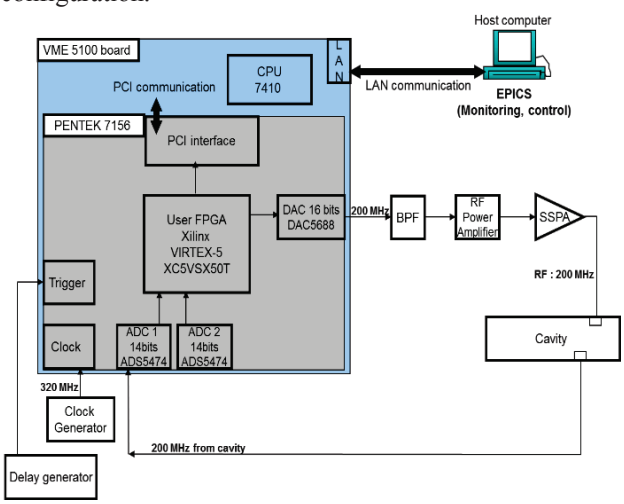

Figure 1: 1 MeV/n RFQ LLRF system configuration.

LLRF ARCHITECTURE

System Configuration

Figure 1 shows 1 MeV/n RFQ LLRF system configuration. The low-level system uses the commercial PMC board which was shown in Fig. 2. The high level system uses the VME5100 board and EPICS system to monitor and control the LLRF system. The output RF signal will be amplified by the SSA to supply the sufficient power RF signal to the RFQ cavity.

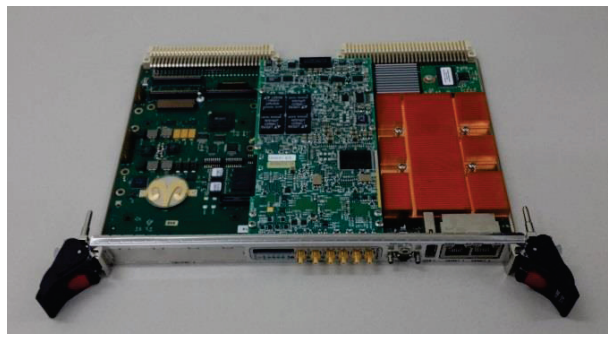

Figure 2: Digital LLRF PMC board and VME board.

Direct Sampling

To minimize the analog components especially analog mixers, this system adopted the direct sampling. The direct sampling avoids the problems related with the analog mixer. In addition, owing to the direct sampling, the LLRF system minimized the budget and the system configuration was simplified. However, the direct sampling has a disadvantage. The ADC (Analog to Digital Converter) clock jitter increases when the clock signal increases the frequency as described in [2]. So we adopted the non-IQ sampling to minimize the negative effect of the direct sampling. The non-IQ sampling will be described in the firmware upgrades part.

Direct RF Generation

Direct RF generation means that LO, IF signals do not need to generate 200 MHz RF signal. The DAC (Digital to Analog Converter) directly generates 200 MHz RF signal. This direct RF generation can simplify the LLRF system configuration and minimize negative effects of the analog components.

In 1 MeV/n RFQ LLRF system case, the output signal frequency source is two digital components as shown in Fig. 3. The DDS (Direct Digital Synthesizer) in the FPGA generates 40 MHz frequency and the NCO (Numerical Controlled Oscillator) in the DAC generates 160 MHz frequency. These DDS, NCO generate the RF signal from the 320 MHz sampling reference clock. Also, the DAC operated as a DUC (Digital Up Converter). As a result, the DDS output frequency mixed with the NCO output frequency in the digital mixer of the DAC so that the DAC can generate 200 MHz RF signal without analog components.

In addition, the DDS in the FPGA can tune 40 MHz RF signal according to the tuning word in the DDS module.

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If possible, the frequency error will be reflected in the DDS module tuning word in the future works [3].

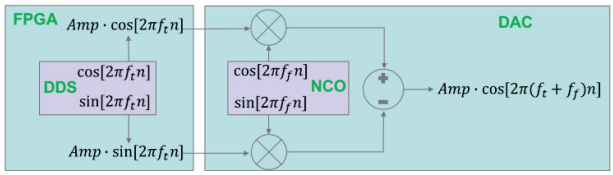

Figure 3: 200 MHz frequency sources of the LLRF system.

FIRMWARE UPGRADES

Non-IQ Sampling

To satisfy the 1 MeV/n RFQ LLRF system configuration, we have to upgrade the processing FPGA control logics of the commercial PMC board. The RF detection technic was upgraded to the non-IQ sampling. The non-IQ sampling technic was developed in 2006 as shown in the [4]. We adopted the non-IQ sampling technic to avoid the problems of the IQ sampling and direct sampling. Non-IQ sampling can avoid the DC offset, noise sensitivity, odd harmonics comparing with the IQ sampling [5]. The non-IQ sampling samples the N samples in the M periods. In 1 MeV/n RFQ LLRF case, N means 5, M means 8. As a result, to detect 200 MHz RF signal with a non-IQ sampling, the ADC requires 320 MHz sampling clock frequency.

I, Q values calculated in the FPGA using FIR (Finite Impulse Response) filter. The FIR filter coefficients are obtained with a least mean square as shown in the [6]. These coefficients are stored in the look up table of the FPGA. The conventional FIR filter in the FPGA IP core calculates I, Q values per M periods as shown in the Xilinx FIR filter datasheet [7]. To increase I, Q values update rate, this LLRF system applied the algorithm as shown in the Fig. 4.

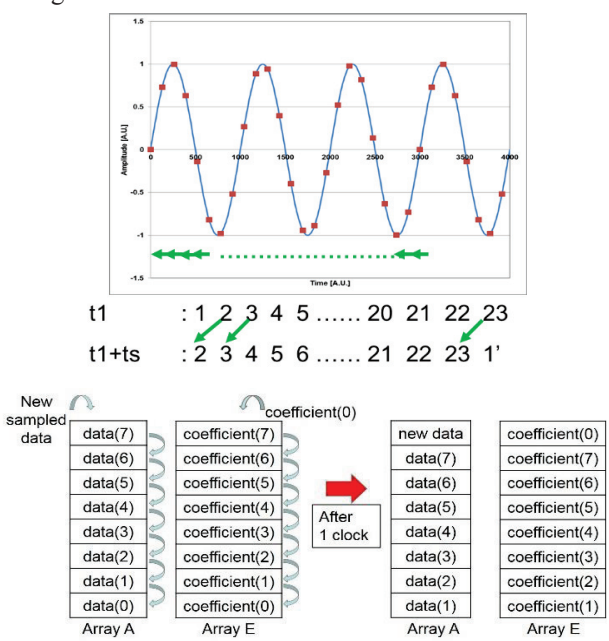

Figure 4: Fast FIR filter update rate algorithm.

Owing to this algorithm, I, Q values updated every 3.125 ns. Without this algorithm, I, Q values updated per 25 ns. As a result, amplitude, phase also obtained per every sampling clock with the CORDIC IP core.

RF Control

Fundamentally, 200 MHz RF signal will be controlled through a PI (Proportional, Integral) feedback control. KOMAC already applied the PI feedback control to 100 MeV proton linear accelerator LLRF control system [8]. PI control will be implemented in 1 MeV/n RFQ LLRF system in near future.

In addition, this LLRF system will track the cavity resonance frequency to simplify the cooling system as shown in Fig. 5 [9]. The strategy is that DAC output signal will play a role as a sampling clock source. However, this strategy is not confirmed that the study about the frequency tracking control mode should be done.

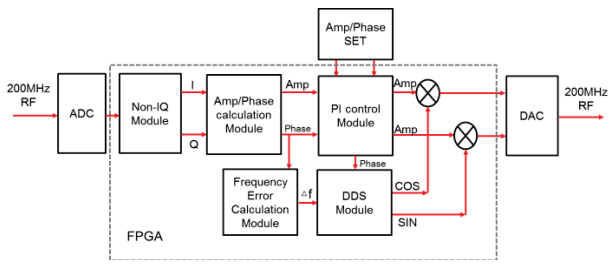

Figure 5: User FPGA control logic.

TEST RESULT OF LLRF SYSTEM

We setup the test bench using dummy cavity as shown in the Fig. 6.

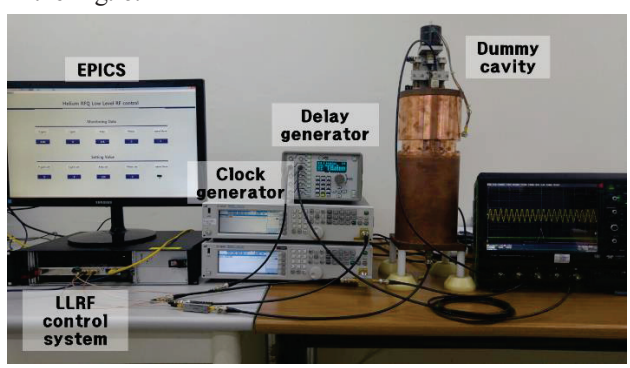

Figure 6: Test setup using dummy cavity.

Until now, we did not tested the PI feedback control that we tested the LLRF system with a RF signal generator. The Digital LLRF control board samples the 200 MHz RF input signal with 320 MHz sampling clock. The output signal of the DAC supply 200 MHz RF signal to the RF signal amplifier. This amplifier supply amplified 200 MHz RF signal to the 200 MHz dummy cavity. As a result, the pickup signal of the dummy cavity monitored through an oscilloscope as shown in the Fig. 7 and the amplitude is monitored through the EPICS system. In the future, if the PI feedback control applied to the LLRF system, the RF control logic will be tested with 200 MHz dummy cavity.

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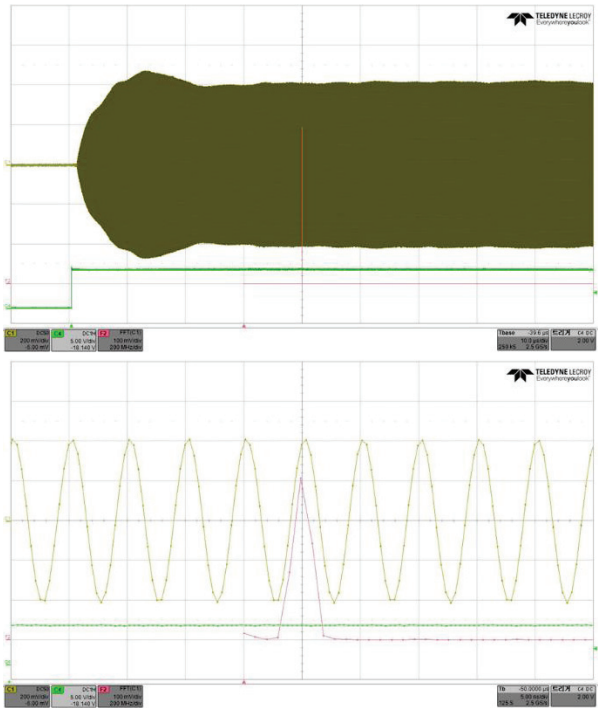

Figure 7: (Upper) 200 MHz dummy cavity pickup signal, (Lower) enlarged waveform of upper picture (CH1 : cavity pickup, CH4 : Gate, F2 : FFT of CH1).

LLRF SYSTEM STATUS

1 MeV/n RFQ LLRF system can detect the 200 MHz RF input signal using non-IQ sampling technique. Non-IQ sampling samples the data using 320 MHz ADC clock. Recent status confirmed that this LLRF system detects 200 MHz input RF signal and calculates the amplitude. Also, this system generates the 200 MHz RF signal without analog components. However, PI control was not tested that additional test should be carried out. The development conducted with the firmware upgrade programming the data processing logics and control logics.

The RF amplifiers, SSAs, arrived at KOMAC site in this year. These SSAs were manufactured at TOMCO (Australia) company. After these SSAs individually tested, the SSAs will be tested connecting the LLRF digital board.

Also, to simplify the cooling system, the frequency tracking mode was considered. However, the frequency tracking mode needs the more study to implement.

CONCLUSION

In this paper, 1 MeV/n RFQ LLRF system test with 200 MHz dummy cavity was introduced. This LLRF system applied direct sampling, non-IQ sampling, direct RF generation and fast FIR filter update rate scheme. These features are related with the RF detection and generation. Also, these features implemented through the firmware upgrades. In the future, RF control logics will be applied. This RF control logics will implement the PI feedback control and cavity resonance frequency tracking control. Also, the future works will include the SSA test.

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