THE DEVELOPMENT OF TUNE MEASUREMENT SYSTEM BASED ON FPGA AT HLSII STORAGE RING

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Abstract

A tune measurement system based on FPGA development board is developed at HLS II. The FPGA development board based on Zynq SOC, have ADC and DAC on board. The FPGA can provide two kinds of signal for exciting the beam: parametric frequency sweep signal and bandwidth limited white noise signal. The FFT algorithms and calculation of tune are running in the ARM CPU. In order to compare performance with the original system which is based on spectrum analyzer, we did experiments with new system based FPGA and original system respectively. The experiments on HLSII storage ring show that the tune measuring accuracy have reached 0.0006 / 0.0001 in horizontal and vertical direction based on sweep frequency of FPGA-based system and the values of tune based on the original system and the FPGA-based tune measurement system are consistent.

INTRODUCTION

Tune is an important parameter in storage ring. The tune is the betatron oscillations number of the particle traveling for one revolution [1]. Since the amplitude of transverse beta oscillations is small, the additional excitation signal is needed. Sweep frequency excitation signal and narrow band white noise excitation signal is frequently used. Different excitation signals have their own advantages and disadvantages and apply to different research conditions of machine [2]. In order to meet the different research conditions of the machine, we need to design a new tune measurement system with two kinds of excitation signals.

THE DESIGN OF NEW TUNE MEASUREMENT SYSTEM

FPGA-based tune measurement system block diagram shown in Figure 1. The tune measurement system includes three parts: the front end module, the digital signal processing module and the host computer. The front module includes BPM, Kiker, front end electronic module which includes low-pass filter, amplifier, attenuator; the block diagram of front module show in Figure 2. Digital signal processing module based on the Red-Pitaya development board whose core chip is ZYNQ-7010 series chip, including ADC, DAC, Xilinx Zynq SoC which integrated FPGA and ARM hard-core processor. FPGA is mainly for the excitation of the signal source and the acquisition of beam signal; ARM is mainly used to transform the beam time domain data which is from RAM of FPGA into frequency domain data and calculate the tune value; host computer is responsible for controlling the acquisition of the start and Stop, sampling length selection, selection of excitation signal type and data storage and waveform display and other functions. FPGA and ARM data through the AXI bus protocol for transmission, ARM and PC data transmission through the network cable. The core part of the system is the data acquisition and processing module.

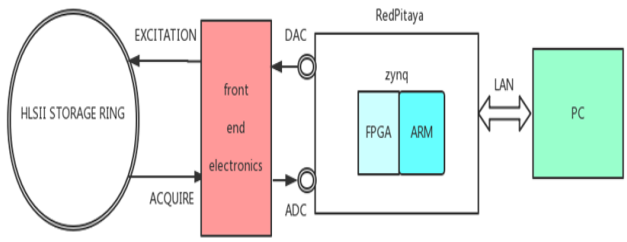

Figure 1: FPGA-based tune measurement system block diagram.

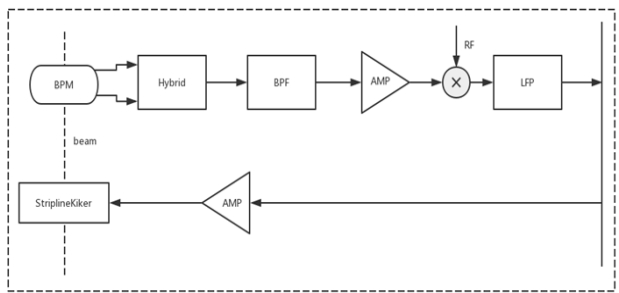

Figure 2: The block diagram of front module.

The simplified schematic inside FPGA is shown in Figure 3. The data from ADC is stored in RAM after decimation and filter which is through finite state machine. The excitation signal output can be selected by status register. The output signal is sweep frequency signal when the register is 0 and bandwidth white noise signal when the register is 1. There are many status registers inside FPGA to control acquire and excitation process. These registers can be read and written by ARM through the physical address.

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ISBN 978-3-95450-182-3

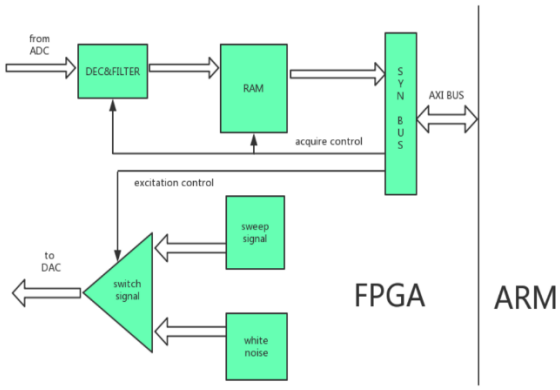


Figure 3: The simplified schematic inside FPGA.

ARM is running on the Linux operating system. ARM processing module includes three parts: communication with the FPGA, data processing and communication with the host computer. According to Linux memory management mechanism, physical addresses and logical addresses can be converted to each other. So ARM can read and write the status registers inside FPGA through physical addresses. Data processing submodule includes FFT and peak amplitude detection.

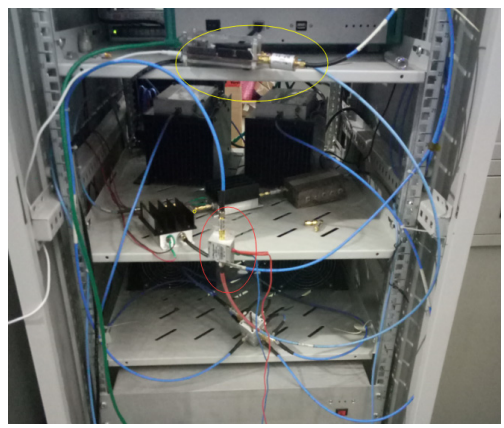
SYSTEM COMMISSION RESULTS

In order to compare performance with the original system which is based on spectrum analyzer, we did experiments with new system based FPGA and original system respectively. The experiment platforms of tune measurement show in Figure 5.The original system and new system use the same front-end module. The excitation and data processing module of original system is Agilent N9000AEP spectrum analyzer. The font OUT in the Figure 4(a) is excitation source of original system, which generates sweep frequency signal. The yellow oval annotation is the FPGA-based board of new system in Figure 4(b).

Original Tune Measurement System Commission Results

The data from BPM are continuously collected 50 times at the beam current of 70 mA. The swept range is set from 2.1 MHz to 3.5 MHz, which covered the tune frequencies in two transverse directions. Figure 5 shows the tune spectrum. Green annotation means the horizontal transverse beta oscillation and red means vertical. Figure 6 shows the measurement results of tune. The average horizontal tune is 0.4470 and vertical tune is 0.3648. The RMS value is 0.0001 in horizontal direction and 0.0004 in vertical direction.

(a)



(b)

Figure 4: The experiment platforms of tune measurement (a) Original system (b) New system.

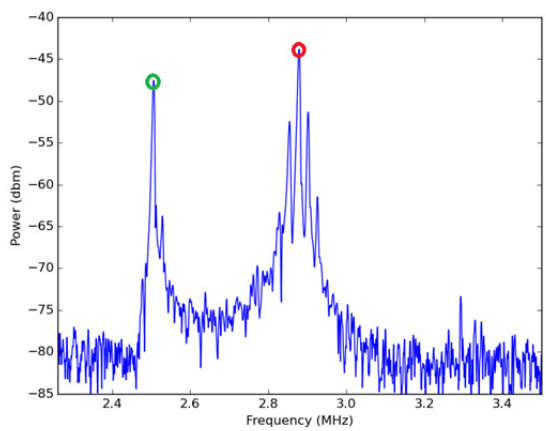


Figure 5: Tune spectrum based on original tune measurement system.

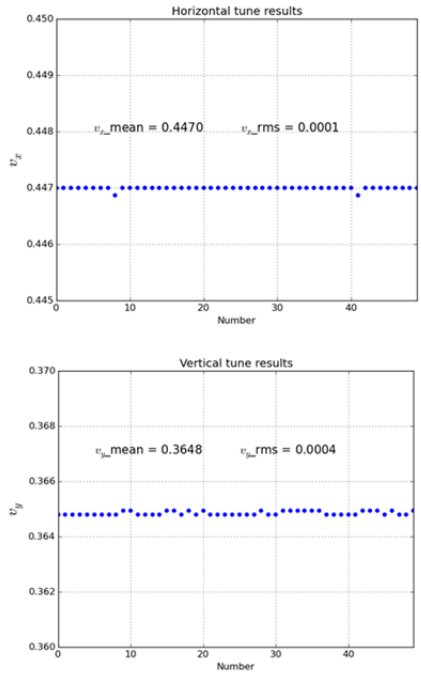


Figure 6: The measurement results of tune based on original system.

New Tune Measurement System Commission Results

Similarly, new tune measurement system send sweep frequency signal and bandwidth white noise signal to the kiker respectively and continuously collected 50 times at the beam current of 70 mA. Two signal type's frequency range is set from 2.1 MHz to 3.5 MHz. Figure 7 shows tune spectrum based on new tune measurement system. Figures 8, 9 show the measurement results of tune.

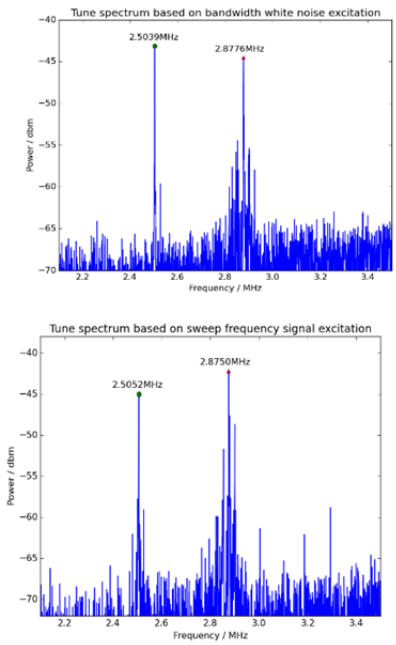


Figure 7: Tune spectrum based on new tune measurement system.

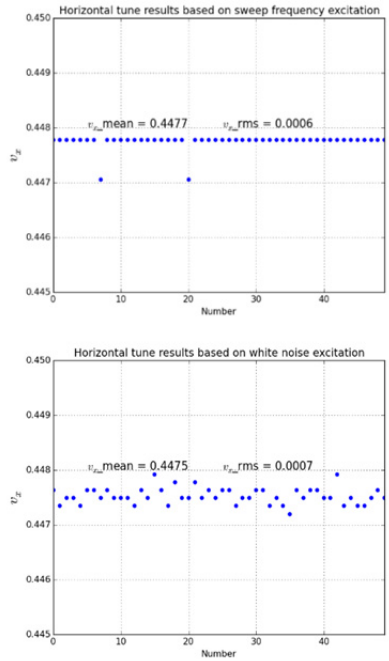


Figure 8: The measurement results of horizontal tune based on original system.

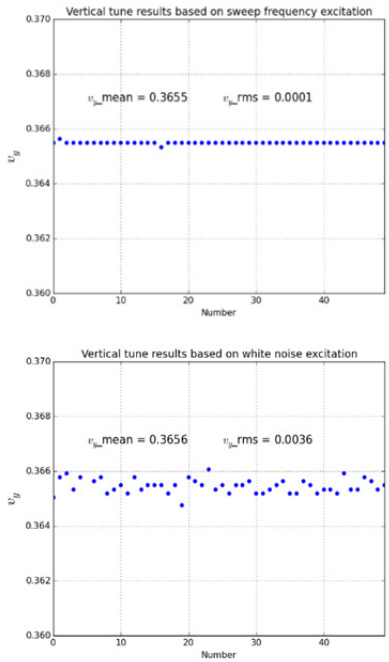


Figure 9: The measurement results of vertical tune based on original system.

CONCLUSION

From the experimental results, it can be seen that the values of tune based on the original system and the FPGA-based tune measurement system are consistent. The measurement accuracy of original system is better than new system. The new system can improve the measurement accuracy by increasing the sampling length and using the Gaussian fitting algorithm and can be programmed online and meet research conditions of the machine.

ISBN 978-3-95450-182-3

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