

## DESIGN OF LCLS-II ATCA BPM SYSTEM \*

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### Abstract

SLAC's LCLS-II is a next generation X-ray FEL that will use a CW 4 GeV superconducting linac with nominal bunch spacing of 1us. It will deliver both soft and hard x-ray FEL to users. In order to achieve the required performance, the SLAC Technical Innovation Directorate has developed a common hardware and firmware platform for beam instrumentation based on the ATCA crate format. We have designed a stripline and cavity BPM system based on this platform that is capable of measuring the beam position at full beam rate. The system will have a dynamic range between 1 pC to 300 pC. This paper will discuss the design of the BPM electronics, overall architecture and performance on LCLS-I.

### INTRODUCTION

The LCLS-II is a CW superconducting linac driven X-ray free electron laser under construction at SLAC. The high beam rate of up to 1MHz, and ability to deliver electrons to multiple undulators (see Figure 1) and beam dumps, results in a beam diagnostics and control system that requires real time data processing in programmable logic. The soft x-ray undulator (SXR) line with 28 undulators optimized for a photon energy range from 0.2 keV to 1.3 keV where as a hard x-ray undulator (HXR) line with 38 undulators is designed for a photon energy range from 1.0 keV to 25.0 keV. (Figure 1). The high beam stability and accuracy needed for FEL generation requires the BPM system to meet the requirements shown in Table 1.

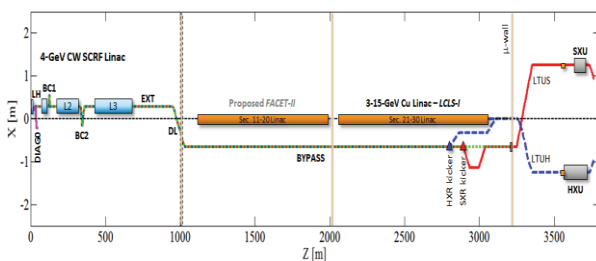


Figure 1: LCLS-II Structure Layout [1].

Table 1: Stripline BPM Operating Requirements [2]

Requirement	Value
Resolution and noise for single pulse measurement, over 10% of the aperture at 10pC	20-30 micron
Dynamic Range	10 – 300pC
Resolution and noise for charge < 10pC	300/Q microns
Maximum drift	5 micron/hour
Maximum electrical offsets	100 micron
Maximum mechanical and alignment offsets	100 micron
Calibration scale error	< 10%
Charge sensitivity	< 5%RMS
2-bunch cross talk	10%
Repetition rate	1MHz

The BPM system provides repeatable transverse beam position data to the Main Control Center and the SLAC global feedback system. In order to meet the stringent requirements, the BPM system performs a self-calibration process between beam pulses.

### SYSTEM DESIGN

The stripline BPMs are installed in the injector, LINAC and transport line sections of the LCLS-II. The motivation for this new design is to have a compact stripline BPM system with high reliability and scalability, while maintaining the performance of original LCLS-I design. The system is realized using the Advanced Telecommunication Computing Architecture (ATCA) platform with a SLAC built advanced mezzanine card (AMC) along with a common carrier FPGA board.

#### SLAC LINAC Stripline BPM Structure

Each BPM has a diameter of 0.87in with a 7% azimuthal coverage. There are four striplines inside the structure, spaced by 90 degrees. The striplines are 4.75in long. To verify each BPM structure does not exceed the maximum acceptable offset, each BPM is tested using a network analyser. The network analyser measures the

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strip to strip coupling coefficient. To increase efficiency a Python script was created to automate the testing process. Equation 1 shows the formula used to calculate the horizontal (X) and vertical (Y) axis offset. PCMM is the measured radius of the BPM structure and S represents the coupling coefficients between electrodes. [2]

$$\left[ \frac{(S_{41}-S_{21})+(S_{43}-S_{23})}{S_{21}+S_{41}+S_{23}+S_{43}} \right] \times PCMM = Xoffset(mm) \quad (1)$$

*Analog Front End/Rear Transition Module*

The analog front end (AFE) has four processing channels, one calibration network, and one clock distribution network for all the JESD clocks (Figure 2)

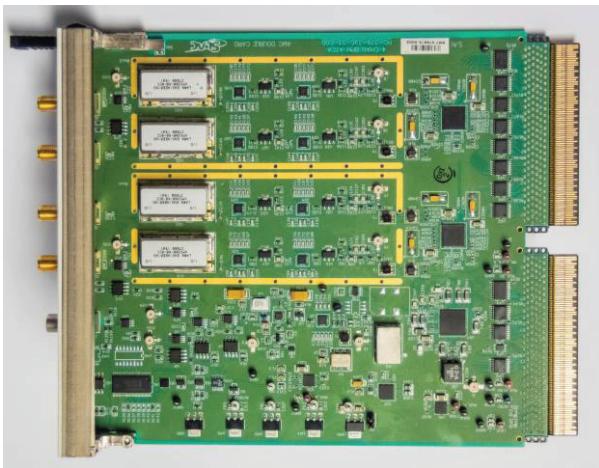


Figure 2: SLAC built BPM AMC.

The original AFE processed the BPM signal at 140MHz (see red curve in Figure 3), which is 35% of the maximum frequency response from the BPM structure. [3] The new AFE/RTM processes the BPM signal at 300MHz, where the signal amplitude is 4.6dB higher in comparison. (Figure 3) The RTM's first stage bandpass filter is a 300MHz bandpass filter with 30MHz or 60MHz bandwidth. When the BPM doublet signal enters the RTM, the filter will create a 300MHz signal with amplitude proportional to the input signal amplitude. To meet the dynamic range requirement and maintain good linear response, there are two digital controlled digitally

attenuators and two RF amplifiers. Each attenuator provides up to 31dB of attenuation in 1dB steps. The first stage amplifier provides 20dB gain, and the second stage amplifier provides 20dB gain. Before the signal is sent to the ADC module, there is a 300MHz anti-aliasing filter with 80MHz bandwidth. After the anti-aliasing filter, the signal is converted from single end to differential using a transformer.

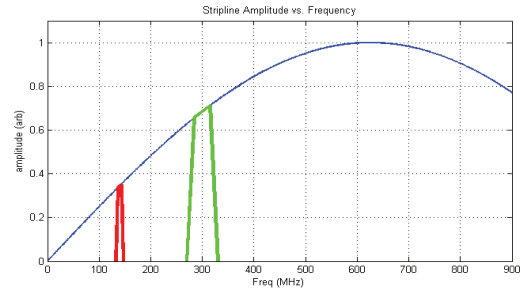


Figure 3: BPM Structure Frequency Response.

The RTM performs a self-calibration process below 1MHz by injecting a 300-MHz tone at a known amplitude into one stripline of each plane. The Y-plane tone calibrates the X-plane via stripline to stripline coupling and the Y-plane is calibrated via injecting a tone on the X-plane. Figure 4 shows the X-plane calibration process. The state-machine inside the common carrier FPGA board controls the switches and RF amplifier to perform the calibration process.

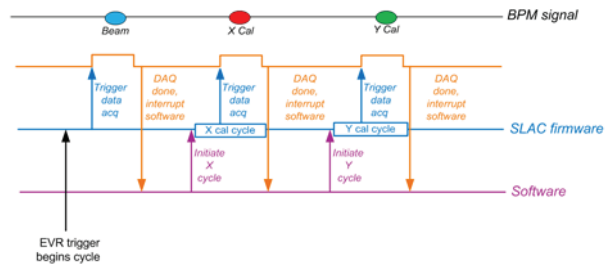


Figure 4: Beam-calibration cycle.

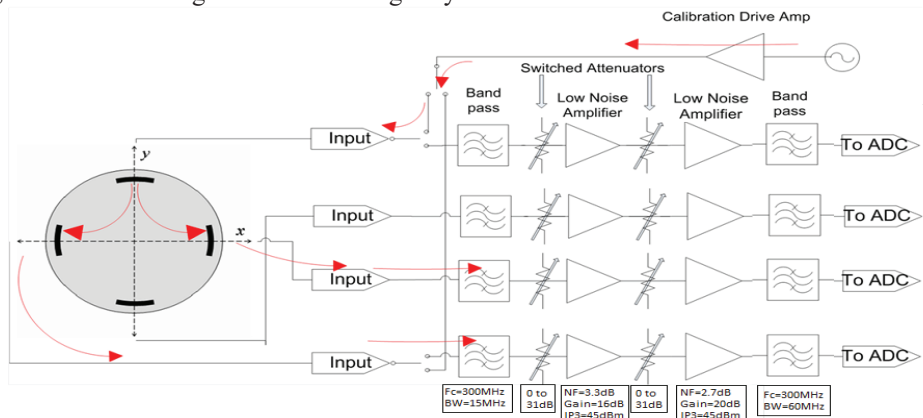


Figure 5: BPM calibration process.

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### Common Carrier Module and ATCA Platform

The BPM system uses a common carrier module contains a FPGA (Xilinx Kintex Ultrascale XCKU040 or XCKU060). It has serial connections to the backplane Ethernet, and to the RTM and AMC cards. JESD204b is used to the AMC cards. The carrier card also contains DC-DC power supplies from the -48V to a variety of voltages used by the AMC cards. A slot of an ATCA crate consists if a carrier card which supports two AMC cards and one RTM card (Figure 6)

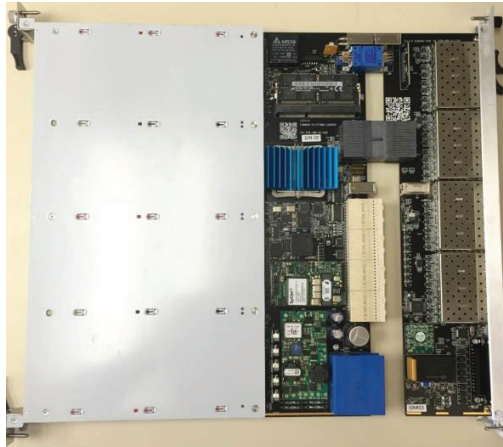


Figure 6: Common Carrier Module.

The ATCA backplane features a dual-star network which provides 10Gb Ethernet connectivity from each carrier module to a switch in slot 1. Timing data is broadcast from slot 2 to all carriers using a proprietary protocol in order to support beam-synchronous data acquisition.

### Graphical User Interface (GUI)

The GUI is created using the EPICS EDM tool. (Figure 7) The GUI displays the calculated X, Y position, calibration waveforms and digitized signals. It also provides user control of the attenuators' attenuation setting.

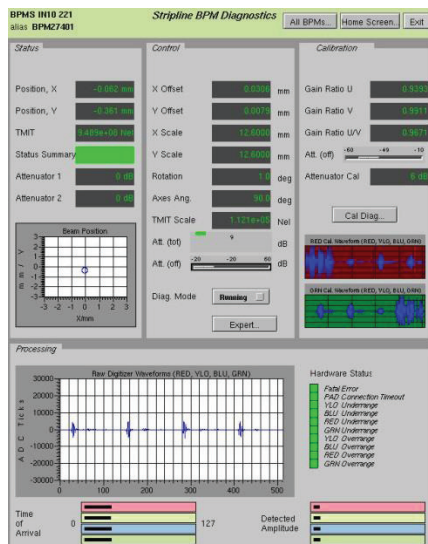


Figure 7: EPICS EDM user interface.

### TEST RESULTS

Three BPMs were installed into the LCLS-I LINAC in December 2016. Since then, the three BPMs have been collecting data like other BPMs. A dynamic range and resolution study was conducted in winter 2016. Figure 8 shows the calculated resolution for the BPMs in the entire L3 section of the LINAC at 10pC bunch charge. The new BPM system was able to produce position resolution between 22µm and 30µm, meeting the requirement of 20-30µm.

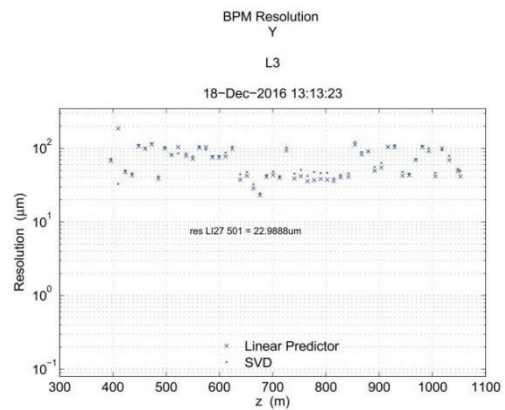


Figure 8: BPM resolution of the entire L3 section of the LINAC.

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- [2] G. R. Lambertson, "Calibration of Position Electrodes Using External Measurements", LSAP Note-5, Lawrence Berkeley Laboratory. May 6. 1987.
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