STABILIZATION OF TIMING SYSTEM OPERATION OF J-PARC LINAC AND RCS

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Abstract

The timing system data (delay value, status, etc.) of J-PARC Linac and rapid cycling synchrotron is managed by a computer. After updating this hardware, we encountered the problem of data corruption in the timing system. Therefore, we added a function to the software for the timing system VME and investigated the cause of the problem. The investigation results showed a problem with the network connected PCI-Express reflective memory. We implemented measures for stabilizing the timing system operation based on this result.

INTRODUCTION

The timing system of J-PARC Linac and rapid cycling synchrotron (RCS) is configured by incorporating reflective memory (RFM) [1][2] so that timing information (beam tag, type, etc.) can be used in the beam monitor and for other purposes. In addition, monitoring and control of the timing system are performed using the same RFM network [3][4].

It has been over 10 years since J-PARC has been operational. Therefore, there are concerns about the occurrence of malfunctions owing to time-related deterioration of the devices in the timing system. Especially, malfunctions of the management computer which is used to monitor and control all timing devices and RFMs used to configure the timing system data network have a significant impact. To stabilize operation of the timing system, updating the management computer was indispensable. Moreover, the RFMs installed in the management computer have been changed from PCI bus type (PCI RFM) to PCI-Express bus type (PCIE RFM).

After updating the computer, RFM data corruption occurred. However, no reports of data corruption had been received by the manufacturers until then. Therefore, initially, data corruption was considered to have occurred because of bugs in the RFM-compatible VME driver used in J-PARC. We investigated the VME driver, but the cause of the problem was not clarified. Moreover, we configured a test bench using only RFMs, and a test involving the transfer of a large amount of data was performed, but the same problem was not encountered in the test. Therefore, we considered that the problem is related to timing system operation and decided to perform the test by using the J-PARC timing system.

In this paper, the contents and the results our cause investigation and those of the measures employed for stabilizing the timing system operation are presented.

TIMING SYSTEM

Configuration

The timing system of J-PARC Linac and RCS is configured by incorporating RFMs. An overview of the timing system configuration is shown in Figure 1. In the Linac and RCS, each RFM network is configured. Because the RFMs for the Linac and RCS (total 2 RFMs) are inserted in a management computer, both RFM networks can be monitored and controlled. The numbers of timing-receive modules and RFMs used in the Linac and RCS are given in Table 1. We found that both RFMs, PMC type (PCM RFM) and VME type (VME RFM), are used in the Linac, and the number of timing-receive modules per VME (RFM) is two. In RCS, only VME RFM is used, and the number of timing-receive modules per RFM is three.

Table 1: Number of Timing Receive Modules and RFMs

	VME crate (CPU board)	PMC type RFM	VME type RFM	Timing-Receive Module
Linac	59	40	19	127
RCS	13	0	13	40

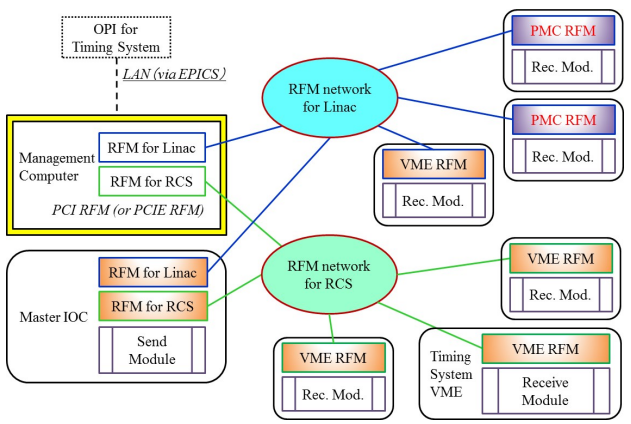

Figure 1: Overview of timing system configuration.

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Parameter Setting Sequence

The parameter setting sequence (operation outline) of the timing system is given below:

(1) Management computer writes timing parameters to RFM.
(2) Management computer sends "parameter read instruction (interrupt)" to all VME.
(3) VME reads parameters for each VME from RFM after receiving "instruction (interrupt)."
(4) VME loads the parameters in own memory and writes the readback value (usually the same as the read parameters).

About (1), because the data size of the timing parameter is 4 bytes × 256 × 8 ch per receive module, it is about 1 MB for the Linac and about 320 kB for RCS.

In the above sequence, (1) and (2) are started by an operator's command, while (3) and (4) are done automatically by VME. Therefore, data transfer of the RFM is caused by the interrupt from the management computer (2) and the readback written by each VME (4). Moreover, data transfer occurs even when each VME writes an increment counter value (counted up in one second period) to RFM.

PROBLEM WITH PCI-EXPRESS OF REFLECTIVE MEMORY

Data Corruption

The problem encountered when using the management computer is that the installed PCIE RFM changes the timing parameters to different values. Here in the parameter setting sequence, when new parameters are not set (when (1) is not performed), the data on the RFM does not change at all (excluding the increment count value). However, according to the investigation, data corruption of the RFM (writing abnormal data) was confirmed by the parameter setting sequence (2) and the actions (3) and (4) accompanying it.

In addition, we tried to identify the cause of data corruption by using a RFM transmission data analyzer. However, all VMEs write readback at the same time because of interrupts, and enormous amounts of data are transmitted instantaneously, so the cause could not be identified using the analyzer. However, when comparing the data before and after the occurrence of data corruption, we found that large numbers of "Reset Node Req" packets flow in the RFM network after the data corruption. However, such packets do not flow in PCI RFM. Therefore, the existence of this packet is considered an indicator of the occurrence of data corruption.

Additional Function of VME Software

To control the amount of data transmitted to the RFM network, the following functions were added to the timing software of VME for efficient investigation.

(i) Enable/Disable increment count
(ii) Enable/Disable readback

Functions (i) and (ii) can be set to Enable/Disable for each VME. In addition, their settings can be adjusted via LAN considering the data corruption of RFM.

Investigation of Cause of Data Corruption

The investigation was performed mainly on the Linac RFM network with multiple VMEs. As shown in the previous section, we investigated the cause of data corruption by checking whether abnormal data is written before and after steps (2) – (4), which is before and after operation (2) and by monitoring the flow of "Reset Node Req" packets by using an analyzer.

First, when step (2) was performed with both functions (i) and (ii) as "Disable" for all VMEs, data corruption did not occur. From this result, it could be concluded that the interruption operation is not a cause, and it was clear that data corruption was caused by the writing of data to RFM.

Next, about PMC RFMs, function (ii) was "Enabled" one by one, number of VMEs executing sequence (4) was increased, and the threshold of data corruption was investigated. As a result, data corruption was confirmed when 23 or 24 (about 47 as timing-receive modules) PMC RFMs were "Enabled." Similarly, the thresholds of data corruption were found when function (ii) was "Enabled" in both cases, "only VME RFMs" and "VME RFMs and PMC RFMs." The result is given in Table 2.

Table 2: Threshold of Data Corruption

	VME (RFM)	Timing-Receive Module
PMC RFM	23 or 24	about 47
VME RFM	16	about 32
PMC and VME RFM	27	about 54

Cause of Data Corruption

We found that data corruption occurs in any configuration as the number of VMEs used for writing data increases. In operation of the timing system, because all VMEs write readback to the RFM by means of an interrupt, the transmission data is concentrated in several to several tens of microseconds (Image of data concentration is shown in Figure 2.). Because the transmission path is included, it is unknown how much data is actually concentrated. However, when concentration of transmission data occurs at a certain scale, it can be assumed that PCIE RFM trouble occurs and the data is corrupted.

Data corruption does not occur when distributing the data concentration by distributing VMEs into four groups and applying time difference processing for writing data at 0, 30, 60, and 90 ms after receiving the interrupts. From this result, we can assume that PCIE RFM trouble occurs owing to data concentration.

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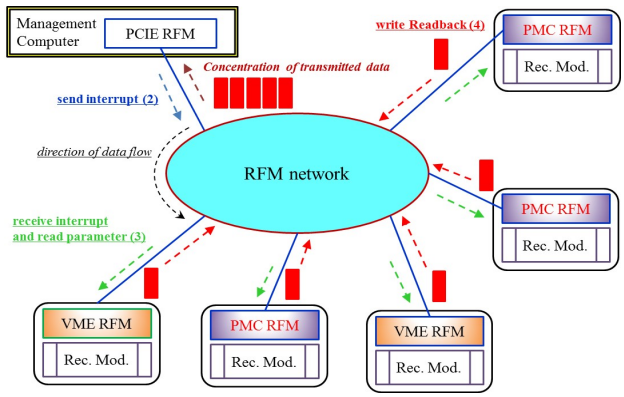

Figure 2: Image of concentration of transmitted data to PCIE RFM.

We reported the result to a Japanese distributor. Moreover, a Japanese distributor checked the occurrence of data corruption. Recently, we have been reported there is a possibility that the problem may occur in the RFM network in which old model RFM and current model RFM are mixedly connected. It is expected that this further cause investigation will be considered by manufacturers.

STABILIZATION OF TIMING SYSTEM OPERATION

Solution of Data Corruption

Because most of the RFMs of the timing system are old models, it is not realistic to replace all RFMs with current models to avoid mixed usage of old and current models. Then, the management computer is forced to use PCI RFM. Therefore, we decided to adopt a PCI-Express - PCI conversion module (3 slot PCI expansion from 1 slot PCI - Express, PE3R made by MAGMA, shown in Figure 3.) to use PCI RFM with a server PC having only a PCI-Express bus. Thus, even in the management computer, which has only PCI-Express bus, it is possible to configure an environment in which PCI-Express is not connected to the RFM network, and operation of the timing system can be stabilized.

Syslog for VME Data

As mentioned at the outset, information of the timing system is transmitted via RFM. Then, when correct information cannot be transmitted owing to RFM trouble, it is difficult to investigate the cause. Therefore, we improved VME software and added a function to record "interrupt (2) log," "read timing parameter (3)," and "written readback (4)" in the syslog server via LAN. This function is useful for ensuring stable operation of the timing system, and it enables early cause investigation when any problem is encountered in the RFM. Experimentally, when data corruption occurred, we confirmed the operation of this function and found that the syslog server logged data indicating whether the VME is reading/writing the correct value.

In other words, it is possible to estimate whether data corruption is occurring in PCIE RFM by using this function.

Figure 3: PCI-Express – PCI converter.

CONCLUSION

In upgrading the management computer, which stabilizes operation of the timing system, we encountered the problem of data corruption when using the PCIE RFM. To solve this problem, we investigated its cause by adding functions to VME software. Based on the results, we found that PCIE RFM trouble occurs owing to data concentration (in the mixed usage of old and current RFMs). In the future, we plan to use the improved PCIE RFM to operate the management computer. However, it may take a long time to develop an improved PCE RFM that solves this problem. Therefore, at present, for stabilizing operation of the timing system, we implemented the following measures: (1) We upgraded the management computer by adopting the PCI – PCI-Express converter. In this way, we can monitor and control the PCI RFM via the PCI-Express bus. (2) Moreover, as a countermeasure against the occurrence of RFM trouble, a function to log the status of each VME via LAN has been developed.

In future, we will improve software such as OPI and further stabilize operation of the timing system.

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