TEST OF THE FEEDBACK AND FEEDFORWARD CONTROL LOOP FOR DIGITAL LLRF SYSTEM OF 1 MeV/n RFQ*

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Abstract

KOMAC (Korea Multi-purpose Accelerator Complex) has a plan to develop a helium irradiation system. This system includes the ion source, LEBT, RFQ and MEBT systems to transport helium particles to the target. The 1 MeV/n RFQ LLRF system was planned to develop the system using fewer analogue components. To minimize the analogue components, the FPGA (Field Programmable Gate Array) was used to implement the logic devices and the direct sampling technique also applied to this digital LLRF system.

In this paper, the FPGA control logics of the LLRF digital board will be introduced. In addition, the digital LLRF system test using 200 MHz dummy cavity will be described. The high power RF amplifier test plan also introduced.

INTRODUCTION

The KOMAC helium RFQ RF system will include a 200 MHz RFQ cavity. This RFQ system requires 1 % amplitude error stability. This RF system is controlled through a digital LLRF board and the RF signal is amplified with the 240 kW SSA (Solid State Amplifier) as shown in Fig. 1. The proposed LLRF system is controlled using only a digital control board and samples the RF signal using the non-IQ sampling technique. In addition, this digital board directly samples the RF signal to detect a RF signal and directly generates a RF signal without analogue components. Furthermore, to implement the feedback control loop, the digital PI controller is applied to the FPGA logic. As a future work, the 240 kW TOMCO SSA system which was already installed in KOMAC building will be test in the near future. The utility constructions including cooling water, 220 Vac distribution and the cable tray installation are under way.

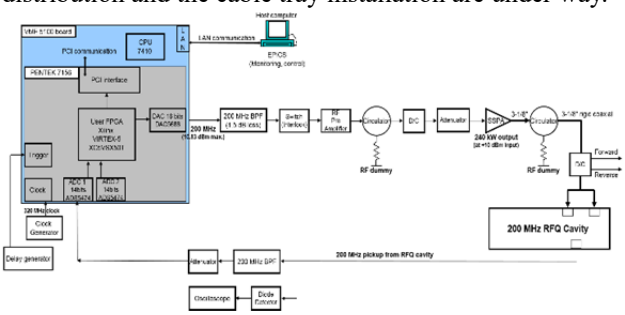

Figure 1: 1 MeV/n RFQ RF system chain diagram.

DIGITAL LLRF SYSTEM OVERVIEW

System Configuration

Fig. 1 shows 1 MeV/n RFQ RF system configuration. The low-level system uses the commercial PMC board (Model 7156) which was manufactured by PENTEK Corporation. This PMC board was originally designed for multi-purpose applications. So that, the KOMAC engineer newly programmed to the FPGA using VHDL (VHSIC Hardware Description Language) to implement the LLRF system through Xilinx 12.3 tool. The high level system uses the VME5100 board and EPICS system to monitor and control the LLRF system. The output RF signal will be amplified by 240 kW SSA to supply sufficient RF power to the RFQ cavity. Also, the circulator between SSA and RFQ cavity protects the SSA from the reflected RF power.

Direct Sampling

To minimize the analogue components, particularly analogue mixers, this system adopted the direct sampling technique. The direct sampling technique avoids the problems related with the analogue mixer [1, 2]. In addition, owing to the direct sampling technique, the LLRF system minimizes the system configuration budget, and the system configuration is simplified. However, the direct sampling technique has a disadvantage. The ADC (Analog to Digital Converter) clock jitter increases when the clock signal increases the frequency. Thus, we adopted the non-IQ sampling technique to minimize the negative effect of the direct sampling [3, 4].

Direct RF Generation & Non-IQ Sampling

Direct RF generation means that LO and IF signals do not need to generate a 200 MHz RF signal. The DAC (Digital to Analog Converter) directly generates a 200 MHz RF signal. Direct RF generation can simplify the LLRF system configuration and minimizes the negative effects of the analogue components usage. To apply the non-IQ sampling and the direct sampling techniques at once, the sampling frequency was determined to operate at 320 MHz. In a 1 MeV/n RFQ LLRF system case, the frequency sources of a 200 MHz output signal are two digital components, as shown in Fig. 2.

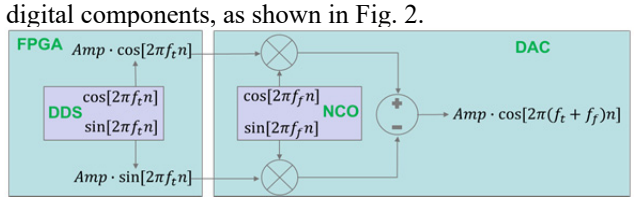

Figure 2: 200 MHz frequency sources in LLRF system.

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The DDS (Direct Digital Synthesizer) in the FPGA generates tuneable frequency of 40 MHz, and the NCO (Numerical Controlled Oscillator) in the DAC generates fixed frequency of 160 MHz. The DDS and NCO generate the RF signal from the fixed 320 MHz sampling reference clock. These relationships are shown in Table 1.

Table 1: Relationships with a Clock Frequency

ADC (Non-IQ)	$\frac{f_{RF}}{f_{sampling}} = \frac{200\ MHz}{320\ MHz} = \frac{5}{8} = \frac{2^0 + 2^2}{2^3}$
FPGA	$\frac{f_{DDS\_out}}{f_{FPGA}} = \frac{f_{DDS\_out}}{f_{sampling}} = \frac{40\ MHz}{320\ MHz} = \frac{2^0}{2^3}$
DAC	$\frac{f_{NCO\_out}}{f_{DAC}} = \frac{f_{NCO\_out}}{f_{sampling}} = \frac{160\ MHz}{320\ MHz} = \frac{2^2}{2^3}$

As a result, the DDS output frequency (40 MHz) is mixed with the NCO output frequency (160 MHz) through a digital mixer in the DAC, and thus the DAC can generate a 200 MHz RF output signal with the usage of BPF (Band Pass Filter), as shown in Fig. 3 [5].

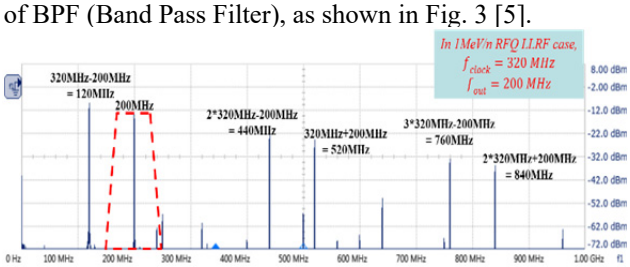

Figure 3: DAC output spectrum without BPF.

Digital PI Controller

To implement the feedback controller, the digital PI controller applied to the FPGA in the LLRF digital board as shown in Fig. 4. The multipliers and accumulator are used in this PI control module. Also, anti-windup technique used in this module to prevent from over driving.

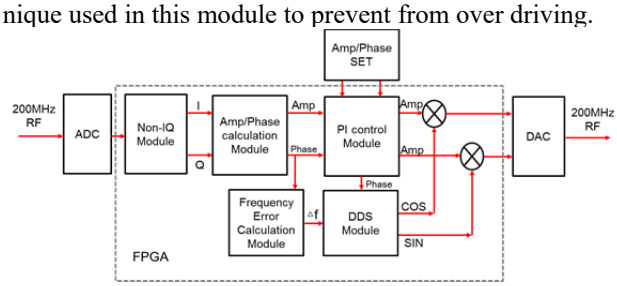

Figure 4: User FPGA controls logics.

FEEDBACK LOOP TEST

Test Setup

To test the performance of digital LLRF, the test bench was configured as shown in Fig. 5. The pulse generator (BNC, 565) output was used as a GATE signal of LLRF system. And the signal generator (Agilent, N5181A) was used as a frequency source of 320 MHz in LLRF system. The SSA (OPHIR, 5300796) was used as a DAC output signal's amplifier to supply sufficient 200 MHz RF power to the dummy cavity which has 3120 unloaded Q-factor.

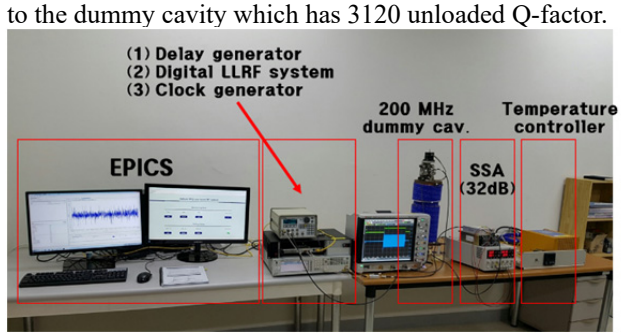

Figure 5: Test bench of digital LLRF system.

Performance of Feedback Control Loop

To verify the feedback loop's performance, the temperature control unit of a 200 MHz dummy cavity operated at non-fixed temperature and the digital LLRF system operated with the open loop and the closed loop either. The temperature variation plays a role as an external perturbation in this experiment. Also, the closed loop test was conducted at 10% duty maximum (100 Hz repetition rate, 1ms pulse width). The orange trend in Fig. 6 indicates the dummy cavity's temperature and the blue trend indicates the amplitude pickup signal of the dummy cavity. From each blue trend line, the shot-to shot stability can be observed. As shown in Fig. 6, the feedback loop controls the amplitude less than 1 % error despite the temperature variation. The performance of feedback loop can be seen easily by comparing the open loop test and the closed loop test.

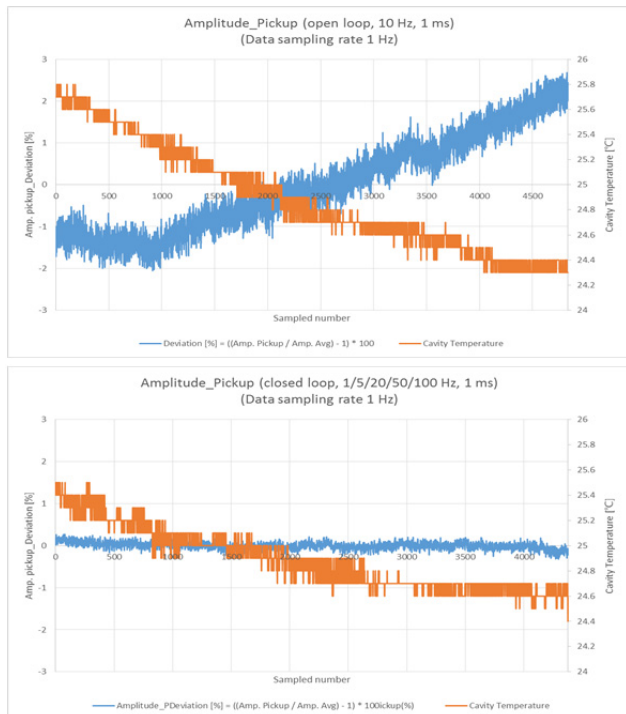

Figure 6: Comparison open loop and closed loop. (Upper) open loop test, (lower) closed loop test.

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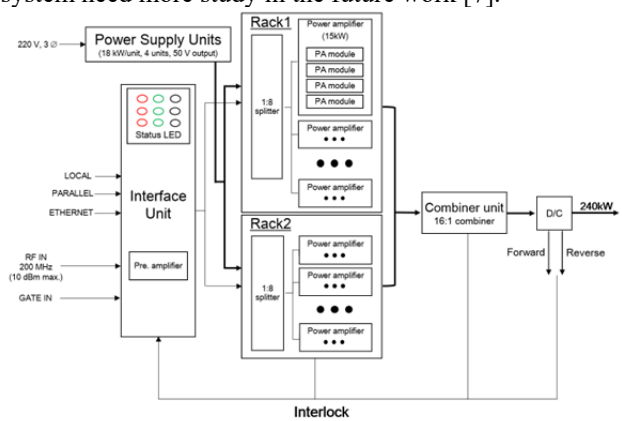
FUTURE WORKS

The 200 MHz, 240 kW SSA (BT240K-DELTA) that was manufactured by TOMCO company will be used as a RF power amplifier in this RF system. The Fig. 7 shows the block diagram of the SSA configuration. This pulsed type SSA which already installed in KOMAC building can generate the 10 % duty RF signal. To operate the 240 kW SSA, the utility installation including cooling water and electrical line is under way. After this SSA individual test accepted in the near future, the digital LLRF system will be added to the RF chain as already shown in Fig. 1.

Another future work related with feedforward controller that was not developed yet. However, the static beam feedforward controller is considered as a feedforward control of this digital LLRF system. The strategy for implementation is utilizing the already implemented feedforward controller. The similar feedforward controller was implemented in the digital LLRF system of the 100 MeV proton linear accelerator [6]. Also, the iterative learning controller which can be applicable in LLRF system need more study in the future work [7].



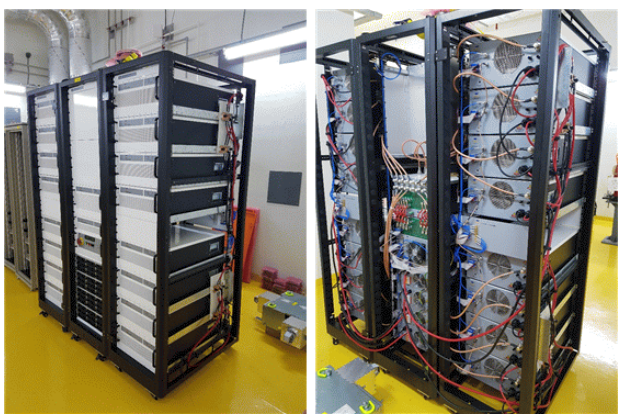


Figure 7: 240 kW SSA. (Upper) block diagram, (lower) picture of SSA located in KOMAC building.

CONCLUSION

In this paper, 1 MeV/n RFQ LLRF system test with 200 MHz dummy cavity was introduced. This LLRF system applied direct sampling, non-IQ sampling, direct RF generation and digital PI controller. These features are related with the RF detection, generation and control. Also, these features implemented through the firmware upgrades and satisfied with the LLRF requirements. In the near future, the 240 kW SSA test will be conducted and the digital LLRF system connected to the RF chain.

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