HIGH EFFICIENCY HIGH POWER RESONANT CAVITY AMPLIFIER FOR ACCELERATOR APPLICATIONS*

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Abstract

Diversified Technologies, Inc. (DTI) designed and built a unique integrated resonant-cavity combined (SSA) for particle accelerator applications, initially focused on Fermilab's Proton Improvement Plan-II (PIP-II). DTI's Phase I SBIR prototype demonstrated high power output at 650 MHz with very high efficiency through Class-E operation. In Phase II, DTI will extend the work by building and testing a 100 kilowatt-class amplifier by combining four of the amplifier modules with associated power supplies.

PROJECT BACKGROUND

This purpose of this project is to design and demonstrate the next generation of cavity amplifiers, to be used for powering future PIP-II accelerating cavities. Many solid-state power amplifiers will be required to power the 650 MHz section of the Linac. The cavities require a minimum peak power of 40 kW per unit and are designed for up to 100 kW CW. This next generation SSA technology must operate efficiently (Class-E) and reliably.

KEY ATTRIBUTES OF DTI'S DESIGN

DTI's SSA design is a radical simplification of high-power, narrow band transistor-based amplifiers, and allows for straightforward scaling to increased power levels (100's of kilowatts) at most accelerator frequencies (Fig. 1). The design directly couples numerous transistors into a low-loss resonant cavity, which operates both as a combiner and as part of the transistor output matching network. A crucial innovation is demonstration of an inherently reliable "graceful degradation" mode of operation, which allows continued operation in the event of even several transistor failures. This is essential for advanced particle accelerator facilities which operate continuously over long periods of time.

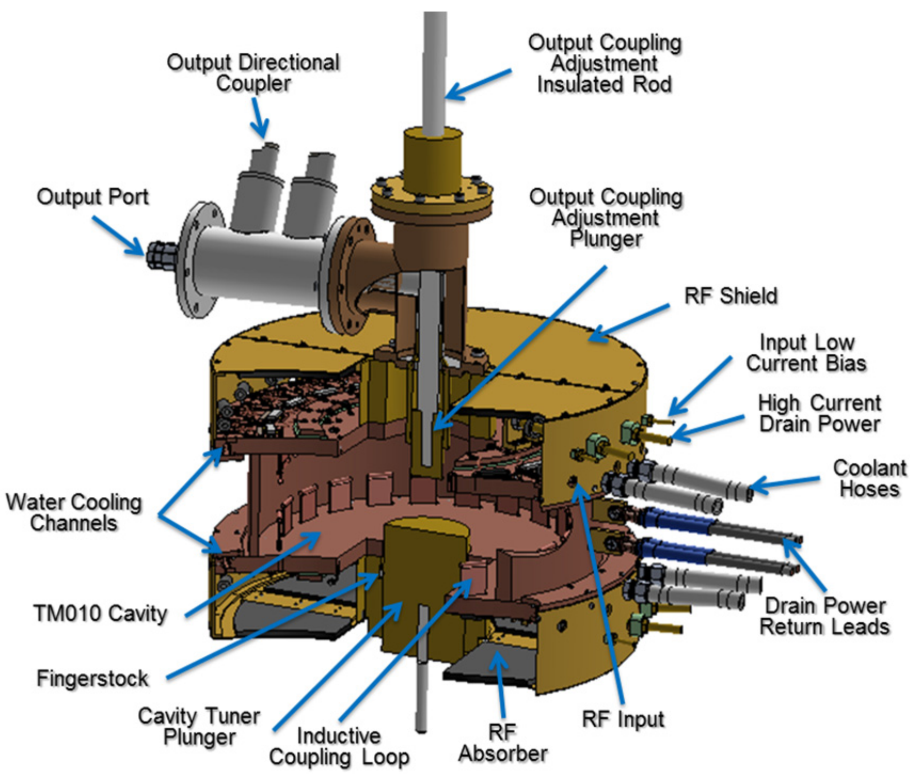

Figure 1: Detailed cut-away view of the integrated resonant cavity amplifier/combiner module.

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A conventional SSA has a complete set of electrical and water cooling connections for every stage, resulting in hundreds of connections for a high power transmitter. DTI's design couples the transistor drains directly to the cavity without first transforming to 50 Ω, avoiding the multitude of circulators, cables, and connectors in a conventionally combined SSA. This construction both reduces the cost of SSAs and significantly increases the power level at which it is cost-effective to employ a solid-state transmitter.

The cavity-coupled SSA built by DTI demonstrated the following key attributes which differentiate it from other amplifiers:

- • Graceful Degradation
- • Simplicity of transistor direct-coupling to cavity
- • High efficiency through Class-E Operation
- • Substantially minimized number of RF, electrical, and cooling connectors.

DESIGN DESCRIPTION

Cavity Combining Overview

The resonant cavity is a well-known means of combining or dividing power. Typically a cavity has a high unloaded Q, so that intrinsic losses can be very low. With heavy input and output loading, the loaded Q is much lower, giving good bandwidth while retaining the intrinsic low conduction losses of the cavity. The specified cavity mode offers a large, well-defined electromagnetic field structure which can be driven simultaneously by many transistors. In principle, various cavity geometry and mode combinations could be used with the cavity-combined amplifier concept. For simplicity, and practical reasons, a cylindrical design (TM010 mode) was chosen for the prototypes, though a more complex coaxial or other structure may ultimately be used for specific products.

The TM010 cavity is driven by circular arrays of loop coupled transistors attached to both end walls (Fig. 2). The output of high power transistors are impedance matched and combined in one step. This power is coupled out into a 3-1/8 inch 50 ohm coax with a single central E-field output coupling probe. The drive signals are coupled to transistors from a similar small resonant cavity divider. Cooling is implemented with parallel water-cooling channels in the end walls under the transistors.

High Efficiency Operation – Class -E

The power amplifier board contains the Class-E output circuitry for each transistor. The output circuit on this board incorporates the harmonically-tuned output matching network for the transistor and interfaces directly to the cavity coupling loop. Harmonic tuning controls the drain voltage waveform to be close to a square wave, rather than a somewhat sinusoidal shape as exists in conventional amplifier (Fig. 3). The square waveform allows a large current conduction angle for the transistor, while simultaneously minimizing V x I losses in the device. This achieves high efficiency and high power in the same cir-

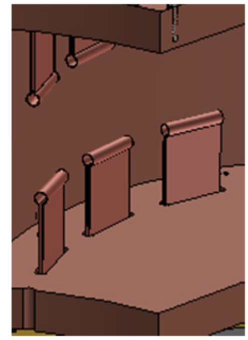

Figure 2: Detailed view of several coupling loop assemblies. Low impedance stripline couples the transistor drains directly to each loop. The combination of this circuitry and the cavity impedance matches to the low impedance of the transistor.

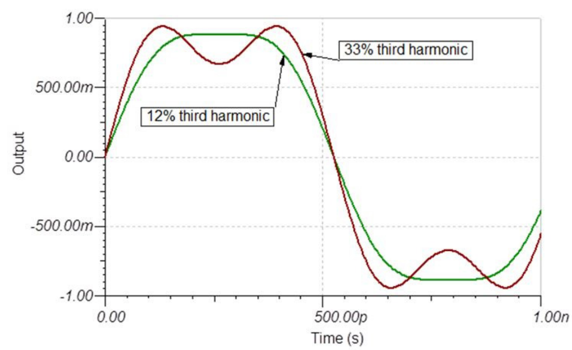

Figure 3: Greatly simplified simulation showing fundamental plus third harmonics for Class-E drain voltage waveforms.

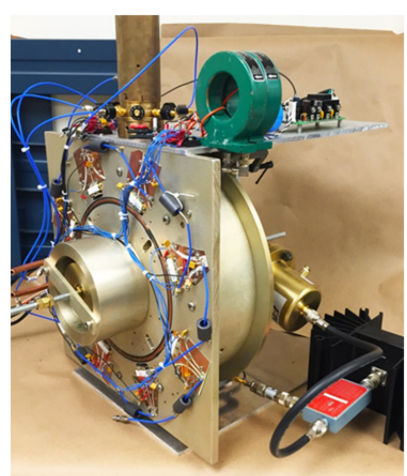

Figure 4: Eight-transistor cavity-coupled amplifier upgraded to high efficiency Class-E demonstrated under Phase I. This cavity, designed for a frequency of 650 MHz, demonstrated 4.5 kW.

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cuit. Class-E is superior to Class-AB (which achieves high linearity at the cost of efficiency) and Class-C (which achieves high efficiency by employing a narrow current (conduction angle) waveform) in efficiency. These conventional methods are ultimately limited by the peak current capability of the device, or by simple R_{DS}-on power losses due to the excessive peak current.

Class-E circuitry approximates a square voltage waveform at the transistor drain by adding 3rd harmonic resonant tuning in the output circuitry. The output combining cavity resonates only at the fundamental, while the drain coupling circuit also resonates at the odd harmonics to make the individual drain voltages a better approximation to square for Class-E high efficiency.

PROJECT ACHIEVEMENTS

Under an internally-funded effort, DTI was able to demonstrate a 650 MHz cavity combiner with an output of 4.5 kW operating in Class-A/B (~40% efficiency (Fig. 4). Modifications to the transmission line, and coupling loop (including the addition of an end-stub) enabled successful high power operation in Class-E (Fig. 5), with ~ 70% efficiency.

FUTURE PLANS

Under the Phase II SBIR effort DTI intends to upgrade the cavity to accommodate 32 transistors, for a power output of ~25 kW. DTI will build a complete transmitter incorporating four of these modules, using a passive combiner to achieve a high efficiency 100 kW-class transmitter (Fig. 6). DTI is also scaling this design to L- and S-bands (1.3 GHz and 3.2 GHz) for related markets.

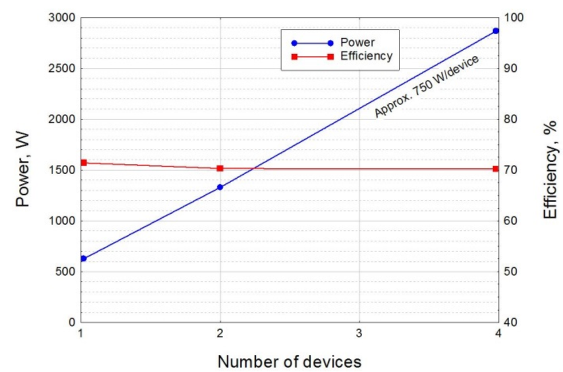

Figure 5: Under this effort DTI demonstrated operation of the cavity combiner at 650 MHz, populated with 4 transistors with ~70% efficiency. Each transistor operated at ~650 V.

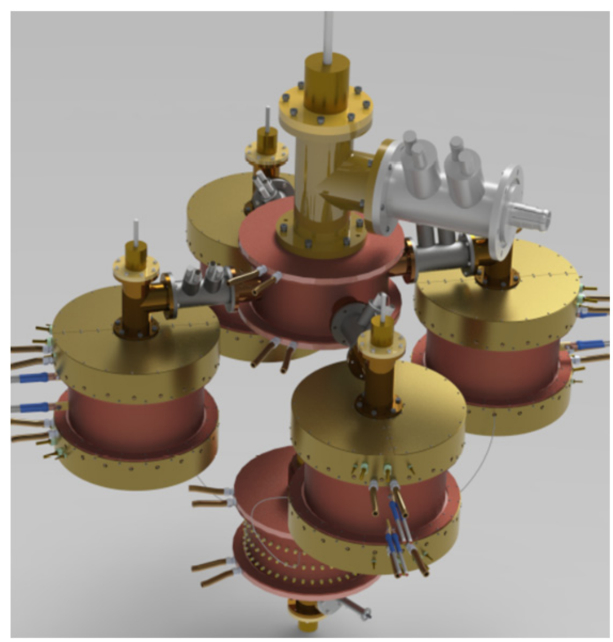

Figure 6: Conceptual layout of a high power solid-state transmitter based on four DTI cavity amplifier modules combined in a passive 4:1 cavity combiner.