PERFORMANCE OF ATCA LLRF SYSTEM AT LCLS*

J. M. D'Ewart[†], J. Frisch, B. Hong, K. Kim, J. Olsen, D. Van Winkle
SLAC, National Accelerator Laboratory, Menlo Park, CA 94025, USA

Abstract

The low level RF control for the SLAC LINAC is being upgraded to provide improved performance and maintainability. The new LLRF system is based on the SLAC ATCA common platform hardware. RF control is achieved through a high performance FPGA based DDS/DDC system. The signal processing is designed to be phase insensitive, allowing the use of modest performance on-board digitizer clock and LO. The prototype LLRF control system was installed and used to operate RF station 28-2 in LCLS-I. Design details and prototype performance results will be presented.

INTRODUCTION

Most LLRF stations at SLAC are from the SLC era and based on CAMAC control hardware. The system is difficult to repair, with limited replacement parts availability. The legacy control system consists of a single sector sub-booster klystron and two racks of CAMAC controls hardware per each of the 8 klystrons. A block diagram of the legacy system is shown in Figure 1. A new LLRF control system has been developed to improve maintainability, reliability, and flexibility.
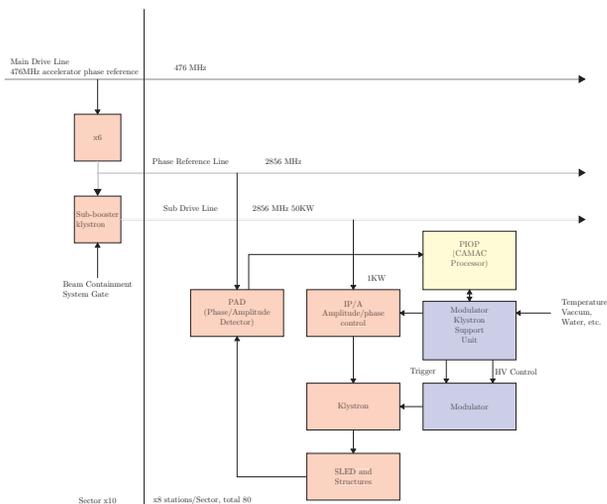
Figure 1: Legacy LLRF.

REQUIREMENTS FOR THE LCLS LLRF UPGRADE

The new ATCA LLRF system will replace the legacy CAMAC controls. The new system must have longevity to last SLAC for the next several decades.

Functional Requirements

The new LLRF system must support an incremental upgrade, thus it must:

- Maintain compatibility with existing LLRF system, including high level applications.
- Maintain compatibility with existing beam containment system (BCS).
- Replace legacy Modulator Klystron Support Unit (MKSU) that protects the high power pulsed klystron and modulators.

RF Requirements

The overall LLRF system is expected to produce < 0.1 degrees RMS phase noise through the accelerating structures. The RF requirements for the digitizing hardware are presented in Table 1.

Table 1: RF Specifications

SPEC	VALUE
Phase noise	< 0.01 degrees 1 MHz BW
Amplitude noise	< 0.01% 1 MHz BW
Phase drift	0.1 degrees
Amplitude drift	0.1%, 1min, 2 degree C
RF channel bandwidth	> 10MHz
RF channel resolution	16 bit resolution
Non-linearity	> 10MHz
Modulator voltage readback	14 bit resolution

DESIGN DESCRIPTION

The new LLRF controls are based on the SLAC ATCA common platform [1]. The SLAC ATCA common platform is based on the telecommunications standard ATCA [2]. SLAC has made this a standard hardware platform for controls and data acquisition. The common platform also includes standard firmware libraries. The firmware libraries provide standard services (communications, timing, etc.) and allow for rapid development of new systems. The system further uses a new solid state sub booster (SSSB) for individual klystron control. A new interlock scheme is incorporated with the ATCA hardware. An overall hardware block diagram of the new LLRF system is show in Figure 2.

SLAC ATCA Common Platform

The SLAC ATCA common platform has been developed for new controls and data acquisition projects at SLAC. Many LCLS II and SLAC mission readiness high performance designs are based on the common platform hardware. A standard installation consists of an ATCA crate and number
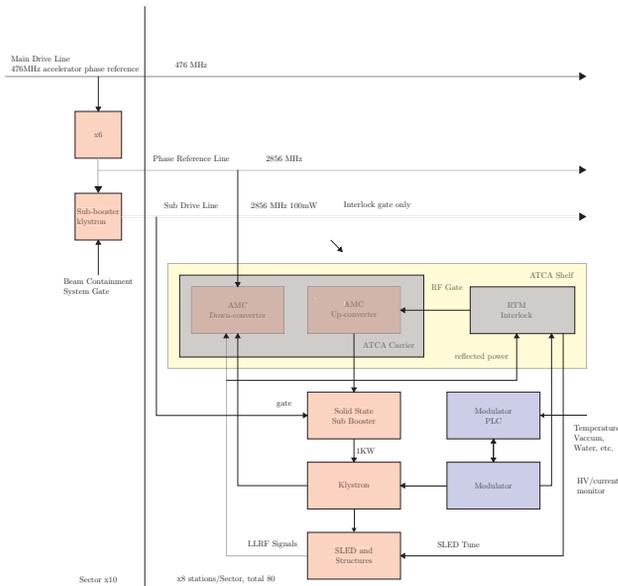
Figure 2: ATCA Based LLRF.

of application AMC carriers. An industrial CPU is used as an IOC and communicates with each carrier via 10 gigabit Ethernet.

RF AMC Cards

Two AMC daughter cards are used for RF processing [3]. Each card has 6 high speed (357 MSPS) JESD204B ADCs. The clock (357MHz) and LO (2771MHz) VCXO are on-board the precision down-converter and distributed to the up-converter card via the SLAC common carrier.

The precision down-converter card has 6 down-converter channels. The 2856MHz RF is downmixed to 85MHz IF and digitized with a high speed (357MSPS) 16-bit ADC. A slow serial DAC is used to control onboard clock and LO VCXOs.

The precision up-converter has 4 down-converters. The up-converter has two additional DC coupled ADCs for sampling modulator voltage and trigger system (EVR timing receiver). The up-converter also has a 16-bit low latency (LVDS) high speed (357 MSPS) DAC. The low latency DAC outputs an IF at 85MHz and that is up-converted to 2856 MHz.

RTM Interlocks

A rear transition module (RTM) has been designed to replace the MKSU for RF interlocks. The RTM monitors beam current, forward and reflected power. The RTM provides external triggers for the SSSB and modulator. It can interlock both triggers and an RF switch to prevent RF output from the AMC cards.

Solid State Sub Booster (SSSB)

The new LLRF system uses a single SSSB per linac klystron. The SSSB is required to produce a 5us 1kW pulse at 120Hz. The SSSB is gated by both the LLRF event system

(trigger) and the BCS system. The RTM provides a 20us TTL gate to enable operation. Additionally the old klystron sub-booster drive line (SDL) is used as an RF BCS gate for the SSSB.

Firmware

The firmware was developed based on the SLAC common platform firmware library. RF processing is designed to be phase insensitive. This allows the AMC cards to run with free running digitizer clock and LO.

SLAC common platform firmware library SLAC has developed an open-source firmware library for integrating common platform hardware. The firmware library includes standard interfaces for timing, diagnostic data, communications, etc. The library allow applications to be rapidly developed and tightly integrated with the LCLS control system. The LLRF application uses the SLAC "amc-carrier-core" firmware as a base platform and only has to implement application specific logic (ex. signal processing).

AMC Card Digital Signal Processing The precision down-converter card has on-board clock and LO VCXO as well as slow DACs to control each. A low bandwidth PLL is implemented to loosely lock each oscillator to the LCLS RF reference. The PLL on the LO VCXO will not by itself meet phase noise requirements. Phase compensation must be done by the RF signal processing chain.

RF Digital Signal Processing The RF signal processing is responsible for phase and amplitude measurement and waveform generation. All phase noise (measured and generated) is additive (relative to the phase reference).

The system uses an 85MHz IF and 357 MSPS ADC. These give an rational IF to clock ratio 5/21. The on-board LO experiences low frequency phase noise thus all phase error measurements are accomplished via common mode phase noise subtraction. Figure 3 illustrates the common mode phase subtraction.
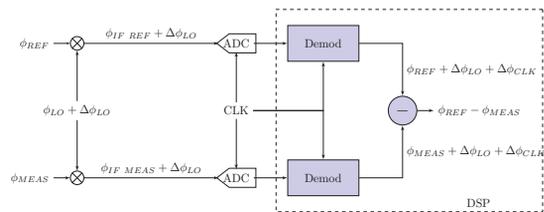
Figure 3: Common mode phase subtraction.

The LO phase noise is also common mode to both down conversion (phase measurement) and up conversion (RF signal generation). A digital phase lock loop (PLL) locks to a single (non phase subtracted) RF reference channel. The quadrature digital PLL output is used to upmix a baseband waveform to IF. The IF is now compensated for the modest phase noise (or free running) LO VCXO. This scheme allows

for overall low additive phase noise signal generation. The signal generation block diagram is shown in Figure 4.
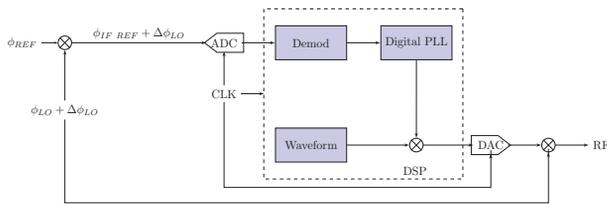
Figure 4: Phase corrected signal generation.

A further requirement is envelop jitter < 100 ps RMS. When externally triggered the sampling clock (2.8ns) has too coarse resolution to meet this alone. One DC coupled ADC can be used to sample a low pass filtered trigger and determine its sub-sample time resolution (w.r.t. sampling clock). This sub-sample timing estimate is then used to arbitrarily interpolate the baseband IQ waveform, achieving « 2.8ns timing resolution.

Finally the firmware must allow for inter-pulse feedback. LCLS uses two phases of the 60 Hz power line to achieve 120Hz operation - timeslots 1 and 4 [4]. The RF signal processing firmware must support timeslot aware inter-pulse feedback. An arbitrary baseband IQ waveform can be specified and timeslot dependent phase corrections can be done by either software or firmware.

Software

The new LLRF software integrates with the existing LCLS control system (EPICS). The software is responsible for FPGA configuration, user display and inter-pulse feedback. Communication with the FPGA happens over UDP and a SLAC reliable communications protocol - Reliable SLAC Streaming Interface (RSSI). The UDP link is used for both configuration and waveform readout. Software can further set arbitrary IQ waveform tables to optimized SLED peak power.

TEST RESULTS

The prototype system was installed in LCLS at sector 28. The station was used in high energy runs in December 2016. The new hardware will continue to operate LI28-2 as LCLS comes back online May 2017.

Lab Results

The AMC cards were tested in a lab setting before installation at sector 28. Brief lab results are presented below.

Measurement phase error Phase error measurements is accomplished by running a split reference signal to two ADCs. The AMC cards digitize each signal at IF (both experiencing the same LO and clock phase noise). The channels are digitally down converted and filtered with a 1 MHz lowpass butterworth filter. A cumulative phase error plot 100 Hz - 1 MHz is shown in Figure 5.
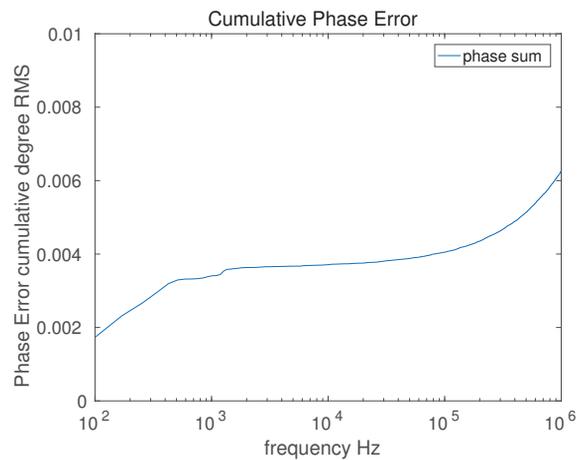
Figure 5: Cumulative measurement phase error.

Measurement amplitude error Amplitude measurement has much less dependency on a low phase noise LO. Each channel amplitude is independently calculated and have < 0.01% RMS noise.

Output phase noise The output phase noise as measured by an Agilent E5052B phase noise analyser is shown in Figure 6. The red line is the phase reference and the blue is the ATCA RF output. The RF output achieves 0.0176 degree RMS phase noise in 100 Hz to 1 MHz at 2856 MHz.
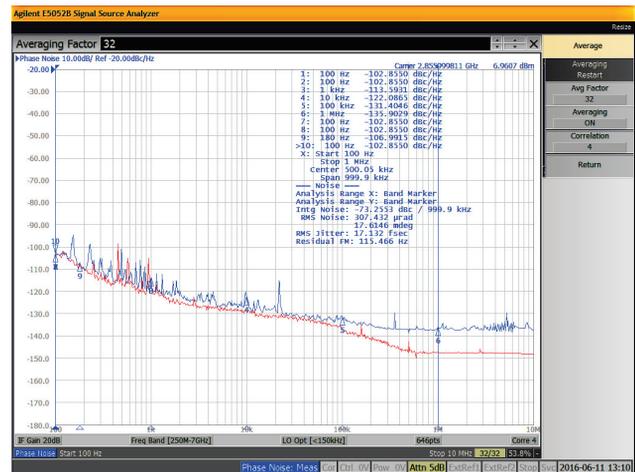
Figure 6: 2856 MHz output phase noise.

Installation at LCLS Sector 28

The entire control system is installed in a single temperature controlled rack in sector 28. The temperature controlled rack provides temperature stability < 2 degree C. The test system is shown in Figure 7.

The complete system was successfully demonstrated at LCLS sector 28 in December 2016. A phase scan of the system going on-beam is shown in Figure 8.

Figure 7: LI28-2 LLRF system installation.
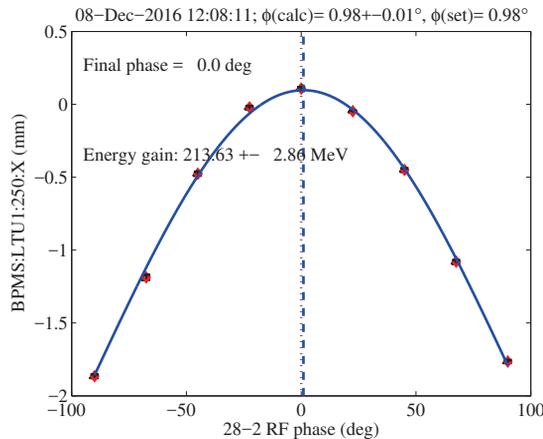
Figure 8: LI28-2 phase scan.

LI28-2 Phase Noise   Phase noise was measured through the RF chain in sector 28. The system was run with timeslot aware inter-pulse feedback.

Phase noise through the RF chain is presented in Table 2.

Table 2: Sector 28 Phase Noise Results

PHASE NOISE	VALUE (degrees RMS)
SSSB Forward	< 0.04
Klystron Forward	< 0.09
SLED Output	< 0.1

Arbitrary Baseband IQ Waveforms   The new LLRF system is capable of producing arbitrary baseband IQ waveforms. An inter-pulse baseband waveform feedback (pulse shaping) was used to improve peak SLED output. The nom-

inal IQ waveforms were shaped to allow for faster phase stabilization of the SLED cavity. Peak SLED output after the first iteration is shown in Figure 9.
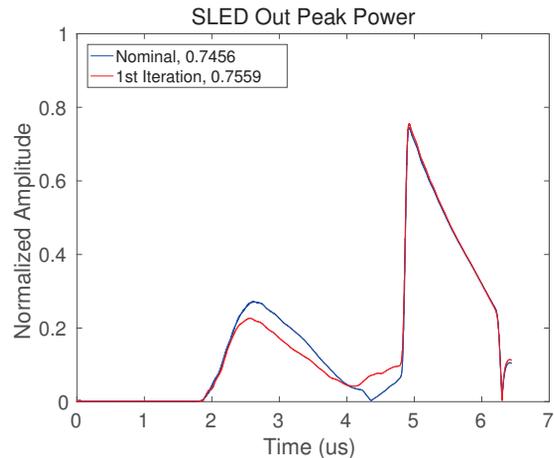
Figure 9: Baseband waveform pulse shaping.

CONCLUSION

A new LLRF system has been designed and demonstrated at LCLS in sector 28. The new system is based on the SLAC ATCA common platform hardware, and uses application specific AMC digitizer daughter cards. Measurement phase noise has been demonstrated to < 0.01 degrees RMS at S-band frequencies. The system is designed to allow an incremental upgrade path for LCLS. Future plans include upgrading the remaining sector 28 stations to the new LLRF design. The remaining installations must work without temperature controlled racks and will experience temperature swings of 40 degrees C. After the sector installation has been complete LCLS will upgrade the remaining RF sectors to the new design.

ACKNOWLEDGEMENT

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