PXIE EMBEDDED CONTROL STATION BASED THE ELECTRIC BREAK-DOWN DATA ACQUISITION AND RF CONDITIONING SYSTEM FOR C-BAND ACCELERATING STRUCTURES USING FOR SHANGHAI SOFT X-RAY FREE ELECTRON LASER (SXFEL)

Ying-Min Li†, Qiang Gu, Wen-Cheng Fang, Jun-Qiang Zhang, Lin Li, Cheng-Cheng Xiao, Jiang-Zeng Gong, Jun-Jie Guo, Zong-Bin Li, Jian-Hao Tan, Meng Zhang, , Zhen-Tang Zhao
Shanghai Institute of Applied Physics, Chinese Academy of Sciences, Shanghai, P.R. China

Abstract

Shanghai Soft X-Ray Free Electron Laser (SXFEL) adopts C-band structure to accelerate the electron to 1.5-GeV. Due to high gradient operation, the electric break-down and structure conditioning problems need to be perfectly resolved. For this purpose, we develop an automatic conditioning control and electric breakdown data acquisition system. The control based on a PXI Express (PXIe) embedded frame and LabView-FPGA technique. The prototype system design, the software programming and hardware test will be introduced. The experiment setup and test results for a low-level signal will be shown.

INTRODUCTION

Recently, 1.5-GeV Shanghai Soft X-Ray Free Electron Laser (SXFEL) is built with many high gradient C-band (5712-MHz) accelerating structures. The accelerating structure is continuously occurred with serious RF breakdown, as begin to work at high gradient with high power which approaches to 50-MW. The RF breakdown directly deteriorated the vacuum, affected more microwave power injecting to structures.

The structure must be working at a stable high gradient. Thus, developing RF conditioning method and studying the mechanism of electric breakdown for the C-band structure will be necessary. To do so we are developing a new automatic RF conditioning system with high power interlock functions for improved safety. The test site consists of an IQ vector modulator, Solid State Amplifier (SSA), klystron, SLED and C-band structure, especially, the appropriate digital control hardware. The core control system is based on a PXI Express (PXIe) embedded frame, and the LabView-FPGA techniques. In this paper, the prototype system design and function principally test were carried on, the software programming and hardware test is finished, the RF streaming for breakdown data storage is on the process.

The C-band structures will operate at accelerating field of 50-MV/m [1], this extremely high gradient frequently results in electric breakdown at the inner surface of copper structure. The oxygen molecule will release from the surface and solid copper may be slightly melt, which reduce the system vacuum and emerge high risk to the scientific research machine. Recently, to study the electric breakdown effects, several accelerator guys put forward to very interested topics [2-3], they are eager to design a useful tool chain for observing and recording these sorts of processes, in order to disclose the mystical questions behind it.

The original industrial control process is based on a general MicroTCA plus with a standard Linux EPICS system, it needs some man power to monitor and operate among the whole conditioning cycle [1]. Due to its low sampling rate around 125-MSa/s, the time resolution cannot be employed for breakdown signal analysis. It needs nanosecond scale time resolution [2]. Thus we choose to use a sampling rate of 1.6-GSa/s system for analysing transient process of the C-band structure breakdown.

SYSTEM DESIGN

Basically, the microwave conditioning system consists of vector IQ modulator, solid state preamplifier, high voltage pulse modulator, klystron, SLED with dual high Q-value cavities, and 81-cell C-band structures, which was designed by SINAP, CAS [1]. They are operated at frequency just 5712-MHz. Also, various waveguides, directional couplers, vacuum equipment and signal monitor device are involved. As shown in Fig. 1.

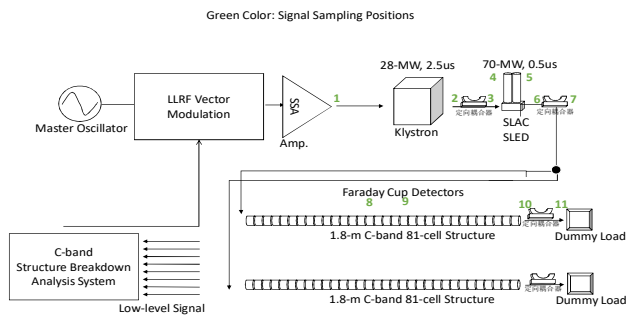

Figure 1: Diagram of the conditioning system for C-band test structures.

To realize pulse compression of the SLED, the input macro-pulse waveform of klystron need to be controlled. Here, we use a vector IQ modulator to change the amplitude and phase of the RF signal within different durations of the macro-pulse [2-4]. Fig. 2 shows the RF modulation signal distribution and IF signal generation for low level

† Corresponding author: liyingmin@sinap.ac.cn

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control test. Here, the master frequency is 5712-MHz, and the local frequency (L.O.) is 5312 or 5512-MHz.

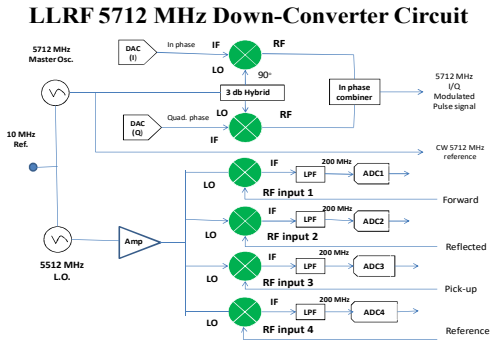

Figure 2: RF Signal Distribution for Low-level Test.

In the RF accelerating structure, during the process of RF conditioning, the RF power input is increasing step by step. The changing rate is almost inversely proportional to the occurring rate of electric breakdown, under certain vacuum level. For example, during 120 seconds, if Breakdown Rate (BDR) is less than 5, and vacuum level is better than $10e^{-4}$ Torr, the input power is increasing by a step value: 0.5 or 1-kW. If BDR is between 5 and 10, the input power is kept constant. If BDR is larger than 10, system immediately cut the power down. Follow the similar rule, LLRF control the input power, judge the balance between the BDR and vacuum, until we obtain the maximum input power for the accelerating structure. Thus the accelerating gradient in the structure could reach to its maximum value. The BDR and the appropriate vacuum level are the figure of merits for injecting microwave power to structure.

HARDWARE IMPLEMENTATIONS

The digital control design is based on a PXIe platform, the communication backplane is a PCIe Gen1 communication standard with 4GB/s system bandwidth. Fig. 3 shows the set-up of the digital control system. Left to the display, is PXIe-1075 chassis. Right to display is frequency down-converter and several signal generators.

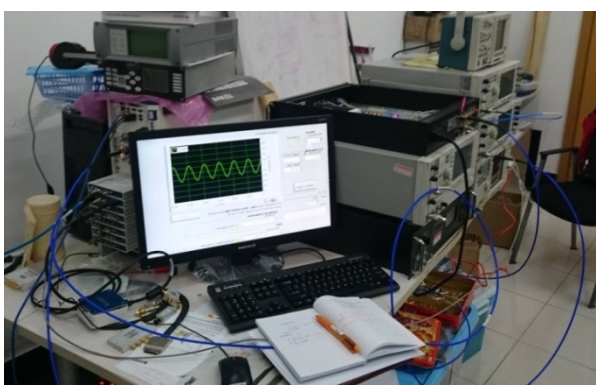

Figure 3: Bench-top set-up for low-level signal test.

The vector modulation process is executed at software defined radio PXIe-5673E transmitter system, the PXIe transmitter is working at 5712-MHz. The high power driving vector signal was generated by this transmitter with waveform storage around 256MB, thus we could generate appropriate RF amplitude/phase modulation envelope for test accelerator.

Data acquisition is operated on NI FlexRIO architecture, and slot-to-slot bandwidth is 1GB/s rate allowable. In chassis, many 1.6-GSpS ADC data acquisition channels were installed to process the low-level signals. The Analog-Digital Converter (ADC) is NI-5772 plus PXIe-7966 FPGA card, which implement the data sampling process. The down-converted pick-up and reflected sampling signal are coming from C-band structure.

A 300-Mbps single ends digital IO with high speed FPGA technologies located within its FlexRIO adapters, it is employed for timing and synchronizations. The digital IO FlexRIO NI-6583 plus PXIe-7961 FPGA card implement the timing and RF trigger for high power system. [5]

Table 1: The Hardware Configuration of PXIe Digital Control System

hardware	model	Specs, performance
Chassis & Backplane	PXIe-1075	17 slots for PXIe
Signal Transmitter	PXIe-5673E	5712-MHz carrier generator
Data Acquisition &FlexRIO module	5772 + PXIe-7966	1.6-Gsps, 352-MHz analog bandwidth, vertical quantization levels at 12 bit. 7966 card has Xilinx v5 FPGA and 512MB memory
Digital IO	6583 + PXIe-7961	300-Mbps bus rate for RF trigger
Host Integrated TCP/IP	PXIe-8135	Communication with MOXA IP to serial server for vacuum interlock

For the RF breakdown research and conditioning cycle of Automation, the main code is implemented with LabView FPGA and LabView RT at a Phar Laps ETS platform system at PXIe-8135 Host. The hardware configuration is shown at Table 1.

VECTOR SIGNAL GENERATION

There are two types pulse compressor operation schemes, they are determined by the amplitude and phase in different duration of the input macro-pulse. One is input with 180° phase flip (step change); the other one is with phase ramp. The former produces a pulse compression with a slope top (sharp tip); the later produces a pulse compression with a flat top. We use a macro-pulse envelope simulator, working with LabView, to generate required macro-pulse waveform. The output of vector IQ modulator drives SSA and klystron, so as to let the SLED generating compressed macro-pulse.

We programmed codes to achieve the pulse modulation in amplitude and phase by using PXIe-5673E. To check

the vector IQ modulator working properly, i.e. ensure SLED perfect flat-top in power magnitude, we use two mathematical functions to generate phase change. The first is to switch 90 degree step at time instance within macro-pulse, and next 90 degree ramp at later time instance within macro-pulse. Fig. 4 shows the joint of a 90 degree step and a 90 degree ramp modulation in phase, but keeps amplitude constant within whole macro-pulse [2].

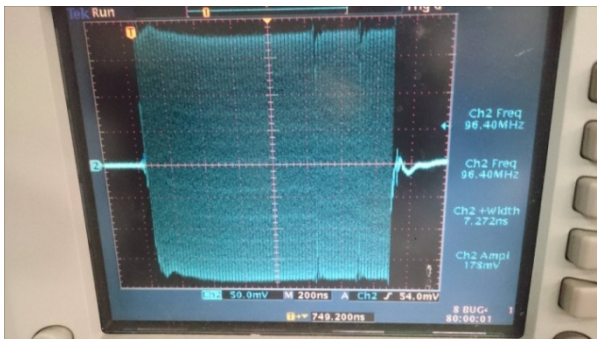

Figure 4: Diagram of the vector modulation signal.

Figure 5 shows the details of the 90 degree change in phase, shown with a Tek oscilloscope.

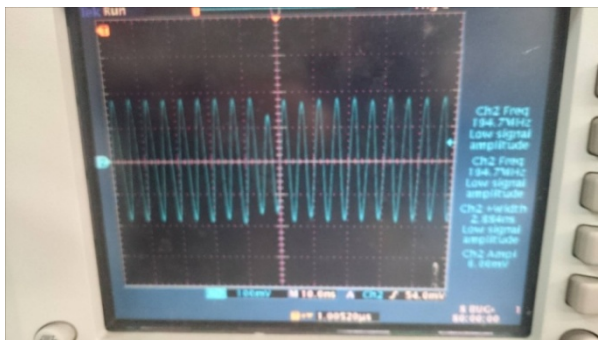
Figure 5: The test signal of the phase 90 degree change.

After obtaining the RF modulation signal, we also use the frequency down-converting circuit with IF frequency 200 MHz and 400 MHz sampling at 800 MSa/s to acquiring the RF modulation signal by NI-5772 card using Labview-FPGA, and to realize the breakdown data acquisition and memory, i.e. RF streaming work.

CONCLUSION

By the initial system designing, set-up assembling, software programming and low level RF testing, we found the experimental setup at bench-top test can work well. The high resolution breakdown waveform analysis is possible. The next step is to realize breakdown data storage in high power test.

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REFERENCES

[1] *Conceptual Design Report of Shanghai X-ray Free Electron Laser(SXFEL) Test Facility*, 2015, www.sinap.ac.cn

[2] J. Benjamin Woolley, "High Power X-band RF Test Development and High Power Testing of the CLIC Crab Cavity," Ph.D. thesis, University of Lancaster, Aug. 2015.

[3] Y. Otake *et al.*, Timing and Low-level RF System for an X-ray Laser, Phys. Rev. Accel. & Beams, 19, 022001, 2016,

[4] Y. Otake *et al.*, "LLRF and timing system for the SCSS test accelerator at Spring-8," *Nucl. Instru.& Methods. In Phys. Research A*, vol. 696, pp. 151-163, 2012.

[5] PXIE hardware manuals, National Instruments, www.ni.com

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