DESIGN OF AN INDUCTIVE ADDER FOR THE FCC INJECTION KICKER PULSE GENERATOR

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Abstract

The injection system for a 100 TeV centre-of-mass collider is an important part of the Future Circular Collider (FCC) study. Due to issues with conventional kicker systems, such as self-triggering and long term availability of thyratrons and limitations of HV-cables, innovative design changes are planned for the FCC injection kicker pulse generator. An inductive adder (IA) based on semiconductor (SC) switches is a promising technology for kicker systems. Its modular design, and the possibility of an active ripple suppression are significant advantages. Since the IA is a complex device, with multiple components whose characteristics are important, a detailed design study and construction of a prototype is necessary. This paper summarizes the system requirements and constraints, and describes the main components and design challenges of the prototype IA. It outlines the results from simulations and measurements on different magnetic core materials as well as on SC switches. The paper concludes on the design choices and progress for the prototype to be built at CERN.

PULSE GENERATOR

Several injection energies are presently being considered for the FCC-hh injection [1]. Nevertheless a very fast system is required to achieve a high filling factor for the FCC; in addition the system must be reliable to avoid mis-kicking beam and consequent damage to downstream equipment. A transmission line kicker magnet, similar to the one used in the LHC injection system, will be used to achieve the short rise times. Thyratron switches are typically used at CERN for injection kicker systems, however they can occasionally self-trigger, have limited dynamic range and cannot interrupt current: hence, for a thyratron, a line type modulator is required to define the maximum duration of current pulse. Another issue is the high voltage (HV) cables used for Pulse Forming Lines (PFLs). New cable is extremely difficult or impossible to source.

To eliminate the aforementioned problems a new pulse generator design is proposed. Recent developments in power semiconductor switches open the possibility of replacement of a thyratron based pulse generator by a pulse generator based on SC-switches: the latter has the ability to interrupt current. However a drawback of SC-switches is their relatively lower ratings for voltage and current, and hence the need for multiple switches in parallel and series to achieve the required values. The inductive adder (IA), presented in [2], presents one possibility for a SC-based pulse generator design. Thanks to the fundamental design of the IA all MOSFET and trigger electronics are referenced to ground, making the triggering circuitry less complex than a pulse generator with floating gate circuitry. A further advantage of the IA is the modular design, which allows built in redundancy and gives the possibility to use identical modules for applications with different requirements. A SC-based Marx generator is also being considered as a pulse generator for the FCC injection kicker system [3].

Table 1: Injection Kicker Requirements

Parameter	Injection
Kinetic Energy [TeV]	3.30
Angle [mrad]	0.18
Pulse length [μs]	2.00
Flat top tolerance [%]	±0.50
Field rise time [μs]	0.43
Voltage [kV]	15.70
Current [kA]	2.50
System impedance [Ω]	6.25

Table 1 shows the FCC injection kicker requirements for a beam energy of 3.3 TeV. To obtain the required field rise and fall times of 430 ns in the kicker magnet, the rise and fall times of the current pulse from the generator need to be <75 ns. A potential drawback of the IA is the output transformer and therefore the risk of saturation of the magnetic core. However with a pulse length of 2.00 μs the requirements for the FCC injection kicker system makes the use of an IA possible. In addition, by employing modulation layers, the flat top tolerance of ±0.5 % is easily achievable with an IA, as these layers allow the generation of pulses with very high stability [4].

Although the available length for the kicker magnets is 150 m, for beam impedance and stability reasons it is desirable to use a significantly shorter length [5], but this increases the current required from the IA. As a compromise a current of 2.5 kA and a magnetic length of ~30 m has initially been chosen: the corresponding magnet deflection angle is 0.18 mrad [5].

INDUCTIVE ADDER PRINCIPLE

The IA consists of a stack of toroidal 1:1 transformer cores: a schematic drawing of the setup can be found in [2]. The rated pulse current of fast switching MOSFETs is typically in the range of 100 to 250 A: hence the primary of each transformer requires multiple parallel branches to provide the required output current of 2.5 kA. The primary windings are located at the outer circumference of the toroidal transformer as shown in [4]. The secondary (stalk) passes through the stacked transformer cores. It encloses the magnetic flux of every “layer” and hence the output voltage is the sum of the output voltages of each layer. The primary voltage per layer is limited by the rated voltage of the SC-switch, which must include a safety margin to ensure good reliability and life time.

To obtain fast rise time the inductance of the primary circuits needs to be low. For this reason the primary winding of the transformer totally encloses the magnetic core. To avoid over voltage across the SC switches when the SC switches are turned off, high voltage freewheeling diodes are included in each primary to provide a path for magnetizing current.

COMPONENTS

Dimensioning the components of the IA requires consideration of many aspects. Realising the required rise and fall times as well as the system impedance of 6.25 Ω are challenging requirements. The characteristic impedance (Z_{IA}) of a layer is defined by the capacitance C_{layer}, the inductance L_{layer} of the coaxial structure and the primary inductance L_p [6]. C_{layer} and L_{layer} are formed by the secondary winding (stalk) and the toroidal primary winding. Important factors are the ratio $\frac{d_o}{d_i}$ of the outside diameter of the insulation to its inside diameter, the layer height l and the relative permittivity ε_r of this insulation material [7]. The parasitic inductance L_p is formed by the primary circuits of a layer. Equation 1 shows the correlation of the values [6]:

$$Z_{IA} = \sqrt{\frac{L_p + L_{layer}}{C_{layer}}} = \sqrt{\frac{L_p}{2\pi\varepsilon l}\ln\frac{d_o}{d_i} + \frac{\mu}{4\pi^2\varepsilon}\ln^2\frac{d_o}{d_i}} \quad (1)$$

In order to achieve the required characteristic impedance with reasonable dimensions, various materials have been considered for the insulation between the primary and secondary windings. The maximum electric field strength, E_{max}, which occurs at the inner diameter (d_i) of the insulation material, must not exceed the breakdown field strength of the insulation including a safety margin. Oil has good insulation and permittivity values. For other insulation materials, e.g. air, the required diameters for the magnetic core end up in the range of 1.5 m which results in very heavy and costly cores [2]. Epoxy has been considered but makes disassembling difficult, for this reason oil has been chosen.

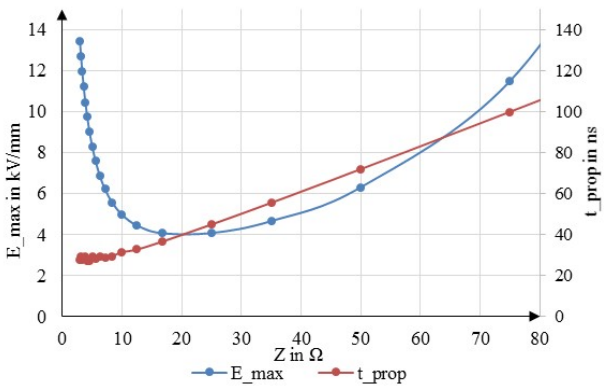

Figure 1: Max. electric field strength versus impedance.

Figure 1 shows E_{max} of the insulation material for a relative permittivity of $\varepsilon_r = 2.7$, outer insulation diameter of $d_o = 108$ mm, primary inductivity of $L_p = 5$ nH and output current of $I_{out} = 2.5$ kA.

It can be seen that E_{max} has a minimum at around 20 Ω. The two way propagation delay of the IA is also plotted in Figure 1: this delay influences the pulse rise time. In coordination with the kicker magnet design a low (6.25 Ω) impedance was chosen: a major advantage is that a given current can be obtained with a relatively low voltage. For the IA a low impedance is demanding from the insulation point of view, but at the same time reduces the length of the stack and hence makes it easier to obtain short currentrise times for a given current.

Magnetic Cores

One of the main components of the IA is the magnetic core. The core will be made from nanocrystalline, tape wound steel and has B-H characteristics which can be somewhat chosen during manufacture. The minimum cross sectional area is defined by the voltage-time integral of a layer and the saturation flux density of the material.

$$A_c = \frac{t_{pulse} \cdot V_{layer}}{\Delta B_c} \quad (2)$$

In Equation 2, A_c is the cross section area of the magnetic core per layer, t_{pulse} is the pulse duration, V_{layer} is the voltage per layer, and ΔB_c the magnetic flux density swing of the core. Equation 2 shows a linear dependence of the core cross section upon the pulse duration. For long pulses the required core cross section becomes very expensive and could exceed the manufacturing capabilities for the cores. Hence the IA is used for pulses of up to a few µs duration. To ensure that the core is not driven into saturation a 40 % safety margin will be considered for the cross section area.

To increase the available flux swing a negative biasing current will be applied to the cores. Biasing means that the working point in the B-H characteristics is set in the third quadrant, before the pulse.

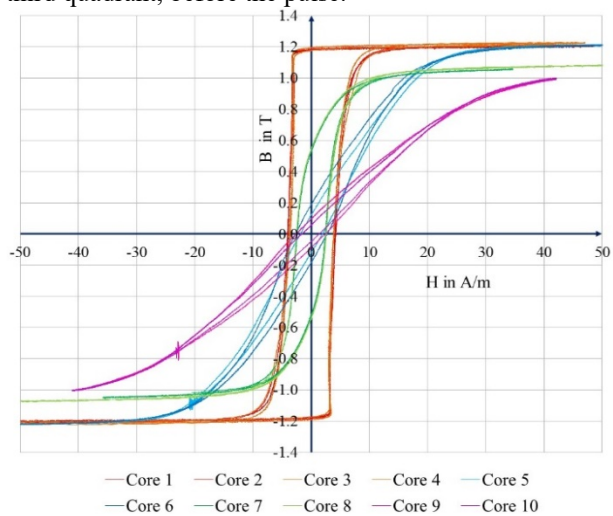

Figure 2: Measured B-H curves of sample cores at 500 Hz.

Sample cores from a number of suppliers and with different B-H curves have been ordered and tested, using

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the technique described in [8]. Furthermore the magnetizing inductance (L_c) as well as the equivalent core loss resistance (R_c) have been measured. Figure 2 shows the measured B-H curves of the sample cores. Magnetizing inductance and core loss resistance, of the different sample cores, are shown in Table 2: cores 1 to 8 have the same dimensions, whereas cores 9 and 10 are slightly smaller.

Table 2: Measured Magnetizing Inductance and Core Loss Resistance of Sample Magnetic Cores

Core	R_c in Ω	L_c in µH	Type of B-H curve
Core 1	55	282	Square
Core 2	50	367	Square
Core 3	65	191	Square
Core 4	75	160	Square
Core 5	150	56	Linear
Core 6	160	42	Linear
Core 7	230	30	Linear
Core 8	200	31	Linear
Core 9	70	28.8	Linear
Core 10	70	28.8	Linear

PSpice simulations with the values shown in Table 2 indicate that all the sample cores are suitable for use in the prototype IA. The simulations show that cores with a square shaped B-H characteristic result in the best performance: even if the core resistance is relatively low the influence is compensated by the higher magnetizing inductance. In addition, the cores with a square shaped B-H curve require a relatively low biasing current.

SC-switches

Many appropriate semiconductor switches, with both turn-on and turn-off capability, exist on the market. IGBTs are available up to several hundred Amps and several kV, but do not have the required fast switching times. Silicon MOSFETs are presently available up to 1200 V and a few hundred Amps: although the switching times are generally fast, the on-state resistance of Si-MOSFETs is still in the range of several hundred mΩ, which causes a relatively high voltage drop for a low impedance system. Silicon Carbide (SiC) MOSFETs are now available with rated voltage of up to 1700 V and pulse currents of more than 100 A. To reach higher current MOSFETs can be connected in parallel. SiC MOSFETs are characterised by a low on-state resistance, usually less than 50 mΩ, and relatively fast switching times. The relatively high voltage rating and low on-state resistance, combined with fast switching, makes SiC MOSFETs the preferred devices for the IA prototype.

SiC MOSFETs with a rated voltage of 1200 V and pulse current values of 190 A or higher have been measured. All tested devices proved capable of switching from 0.5 % to 99.5 % in less than 40 ns, for low currents: measurements for high currents are planned. An important factor to maximize the switching performance is the gate driver, and various drivers are being evaluated.

Pulse Capacitors

The pulse capacitors require a high capacitance to realise the required pulse current and duration with low droop: thus high energy density is desirable. At the same time the dimensions of the capacitor should be kept small to realize a short layer height, to keep the stack length and hence delay low. In addition, the inductance of the primary circuit is influenced by the parasitic inductance of the capacitor itself. To obtain high energy density with low inductance, custom made sample capacitors were ordered and tested. The parasitic inductance of the capacitors was measured together with its series resistance, using the technique described in [9]: results are shown in Table 3. The preferred capacitor, for its low inductance and relatively high voltage rating and energy density, is labelled Cap1.

Table 3: Measurement Results for Capacitor Samples

Type	Cap1	Cap2	Cap3	Cap4	Cap5
C in uF	25 ±10%	25 ±10%	25 ±10%	30 ±10%	35 ±10%
V in V	1500	1300	1100	1100	1100
L in nH	28	30.6	31.1	39.4	35.5
R in Ω	0.32	0.27	0.22	0.28	0.26
Ed in J/cm^3	0.274	0.212	0.166	0.182	0.212

In Table 3, *C* is the capacitance, *V* the rated voltage, *Ed* the energy density, and *L* and *R* are the measured parasitic inductance and resistance, respectively.

CONCLUSION

Design choices for the prototype IA will be based on test results. After the components tests are completed the prototype will be assembled and tested based on the requirements outlined in this paper: the foreseen parameters are shown in Table 4.

Table 4: Design Parameters of the Prototype IA

Parameter	Unit	Value
Nr. of constant voltage layers	-	21
Nr. of modulation layers	-	2
Nr. of branches per layer	-	24
Insulation inner diameter	mm	103.4
Insulation outer diameter	mm	108
Insulation thickness	mm	2.3
Insulation relative permittivity	-	2.7
Characteristic impedance	Ω	6.25
Voltage per layer	V	960
Current per branch	A	105
Core cross section area	cm^2	20.6
Core height	mm	30
Layer height	mm	40
Capacitance per branch	µF	25
Output voltage	kV	15.62
Output current	kA	2.5

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