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FAST ORBIT CORRECTOR POWER SUPPLY IN MTCA.4 FORM FACTOR FOR SIRIUS LIGHT SOURCE

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Abstract

A novel fast orbit feedback (FOFB) hardware architecture has been pursued at Sirius, where fast orbit corrector power supplies share a common crate with BPM and feedback processing electronics. It aims at minimizing the overall latency of the control loop while leveraging the available crate infrastructure. This paper describes the design principles, electronics implementation and first prototype results of Sirius fast orbit corector power supply.

INTRODUCTION

Since its early design phase, the Sirius project has targeted the maximization of the orbit feedback closed-loop bandwidth. This guiding principle led to the design of dedicated high bandwidth vacuum chambers, magnets and power supplies for the fast orbit correctors. Likewise, a low actuator delay[1] was pursued so as to have a negligible contribution to the overall FOFB loop latency.

In addition to the goal of achieving extreme dynamic response performance, the fast correctors' power supplies were conceptualized to make full use of the hardware infrastructure of MicroTCA.4 crates already in place for BPM and FOFB controller electronics, such as enclosure, DC power, forced air cooling, CPU and control software, synchronization, point-to-point multigigabit connectivity and remote hardware management capabilities.

These two main principles led to the development of a MicroTCA.4 Linear Amplifier Rear Transition Module (RTM-LAMP) (Fig. 1) containing digitally-controlled current source power supplies for fast orbit correctors. The RTM-LAMP module is an open hardware design made publicly available [1].

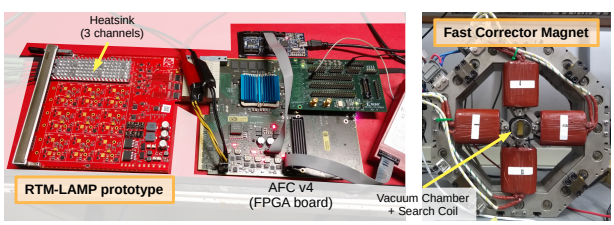

Figure 1: RTM-LAMP and fast corrector prototypes.

REQUIREMENTS

Building on a well-known concept used in other light sources, Sirius will operate with two separate orbit feedback loops [2]. While the Slow Orbit Feedback (SOFB) system accounts for large and slow orbit distortions (spectral content below 1 Hz), for instance storage ring misalignments, ground motion, thermaly-induced orbit drifts and slow changes of insertion devices (IDs) parameters, the FOFB system will focus on mitigating smaller orbit disturbances at the light source points, mainly generated by magnets vibration, power supplies' ripple and fast changes on ID parameters.

The 100 mm-long fast corrector magnet has a FeSi core made of 0.5 mm laminations and 56-turn windings providing up to 30 µrad deflections on Sirius's 3 GeV electron beam. It combines both horizontal and vertical plane corrector coils into a single core and is placed around dedicated 0.3 mm-thick stainless steel vacuum chambers.

Each storage ring sector has 4 fast correctors per transverse plane (8 coils), totalling 80 fast correctors (160 corrector coils). Out of this number, 10 correctors (20 coils) adopt a 45°-rotated configuration to avoid collision with photon beams. The rotated correctors have higher inductance and smaller full scale current.

A resolution better than 1.5 nrad_{RMS} within a 1 kHz bandwidth is required. This number can be translated to a current noise spectral density (NSD) upper bound already taking into account the noise attenuation provided by the FOFB loop. Table 1 summarizes the main power supply requirements.

Table 1: Fast Orbit Corrector Power Supply Requirements

Parameter	Value
Power Consumption	36 W (all channels)
Number of Channels	≥ 8
Output Current (bipolar)	1 A (standard) 0.75 A (45°-rotated)
Bandwidth (1% full-scale)	10 kHz
Slew Rate	0.5 A/ms (standard) 0.375 A/ms (45°-rotated)
Total Delay	5 µs
Noise Spectral Density	$1.5\ \frac{\mu A}{\sqrt{Hz}}$ ($f \geq 1$ kHz) $1.5\ \frac{\mu A}{\sqrt{Hz}} \times \frac{1\ kHz}{f}$ ($f < 1$ kHz)
Crosstalk	−60 dB
Load Resistance	1 Ω (max.)
Load Inductance	3.5 mH (standard) 6.2 mH (45°-rotated)

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[1] The power supply delay is herein defined as the elapsed time between issuing a current setpoint at the FOFB controller and having the earliest voltage update at the magnet coils' terminals as dictated by the current feedback loop.

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SYSTEM ARCHITECTURE

The power supply board was designed as a MicroTCA.4 Rear Transmission Module (RTM). It has predefined interfaces mandated by the PICMG standard [3]. The board provides application-specific peripherals such as ADCs, DACs and amplifiers as well as health monitoring sensors. Data processing and control of such peripherals must be provided by an FPGA located on the front AMC board. The AMC board plays three distinct roles: (1) current feedback controller of each power amplifier channel; (2) BPM data concentrator; and (3) distributed FOFB controller for one Sirius storage ring sector. It is connected to neighbor (or central) FOFB controllers by multigigabit fiber links.

ELECTRONICS DESIGN

The RTM-LAMP is composed of 12 channels, leaving 4 spare channels for future upgrades. Each channel consists of a DAC converter, a Class AB power amplifier stage, a current sensing shunt resistor, an instrumentation amplifier and an ADC.

The power amplifier stage is built with two bridge-tied OPA569 rail-to-rail power amplifiers in order to allow a bidirectional current output using a single positive power supply.

Each channel should supply up to ±1 A and satisfy the small signal minimal current slew rate of 0.375 A/ms given an inductive load of 6.2 mH:

$$\Delta V \geq 6.2\,\text{mH} \times 0.375\,\text{A/ms} = 2.325\,\text{V} \qquad (1)$$

The MicroTCA.4 specifications limit the maximum power consumption for RTM boards to 36 W when sourced from an AMC board. Only 32 W are left after considering the power consumption for the auxiliary digital and analog circuitry (ADCs, DACs, instrumentation amplifiers, etc). With a target efficiency of ≥ 90% for the buck converter, 28.8 W are available to the power amplifiers. The OPA569 amplifier requires a minimum of 2.7 V to operate, so when using all 12 channels at 1 A each an external 12 V supply is necessary. For now, only 8 channels are required, so the power amplifiers can be supplied with 3.6 V, giving ±3.4 V output capability when accounting for the OPA569's output swing.

An efficient buck regulator capable of delivering up to 12 A at output voltages ranging from 2.7 V to 5 V and an input voltage of 12 V was necessary. For this task the ADP1850 buck controller was selected, together with high efficiency MOSFETs and power inductors. The ADP1850 has two independent outputs, channels 0-7 where connected to one of the power rails, channels 8-11 to the other. This arrangement adds the flexibility of using different voltages for each channel group, allowing a better trade-off between the power consumption and performance.

PROTOTYPE VALIDATION

Dynamic Response

The prototype was tested on a NATIVE-R2 crate using an AMC FMC Carrier v4 (AFCv4) as the FPGA board. The current feedback loop was implemented on the FPGA by reusing an open source PI controller design [4]. The loop update period is 0.95 µs, the same as the ADC conversion and DAC update rates.

Initial open loop experiments demonstrated a delay from setting a DAC value to the corresponding change on the amplifier's output voltage to be around 3 µs, which allowed tuning the PI to reach 13 kHz tracking bandwidth wihthout overshoot (phase margin > 70°). For comparison, Fig. 2 shows four transfer functions: (1) measured mangetic field penetration on vacuum chamber; (2) measured magnetic field for current variations on the fast corrector magnet (standard coils configuration); (3) desired power supply current response; (4) target overall FOFB actuactor response. The transfer functions (1) and (2) were measured employing a Keysight 33521A waveform generator and a DSOS104A oscilloscope to sweep and acquire sine waves of various frequencies. The magnet current was driven by an all-analog RTM-LAMP design validation board (DVB) that had been priorly deisgned to validate the power amplifier. The magnetic field at the center of the magnet was measured by observing the emf on a 100 mm-long 36-turn search coil. A frequency-dependent $j\omega$ factor and an arbitraty DC gain were artificially applied to the magnetic field frequency response in order to compensate for the search coil dynamics.

The vacuum chamber response shows excellent agreement with a 25 kHz first order transfer function, while the combined response of the chamber plus the magnet reaches the −3 dB point at around 15 kHz.

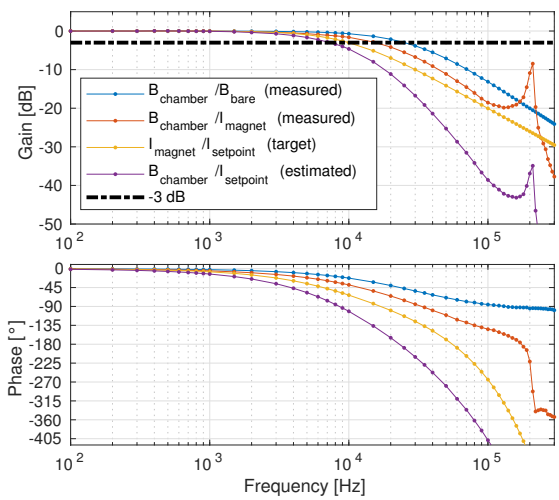

Figure 2: Frequency response of FOFB actuator susbsystems.

Figure 3 shows in time domain the achieved performance of the RTM-LAMP for a 1% of the full-scale step on a 5.9 mH and 1.18 Ω test load. The response is compared to

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that of an ideal 10 kHz first order system with 5 µs delay, i.e., the performance target. At the beginning of the step, the voltage setpoint which is applied to the power amplifier is correctly clamped by the controller's anti-windup logic and avoids overshooting. One can note that the step response requirement is closely met.

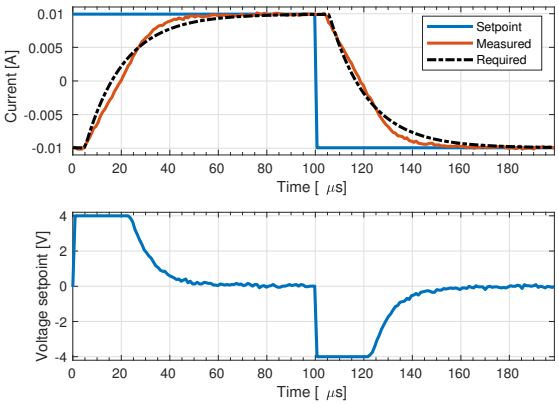

Figure 3: Step response at 1% of full-scale.

Figure 4 shows the worst-case scenario for dynamic response, which is dominated by the load inductance. As before, the controller is shown to be robust enough to avoid overshooting despite the long period under voltage saturation and amplifier non-linear effects.

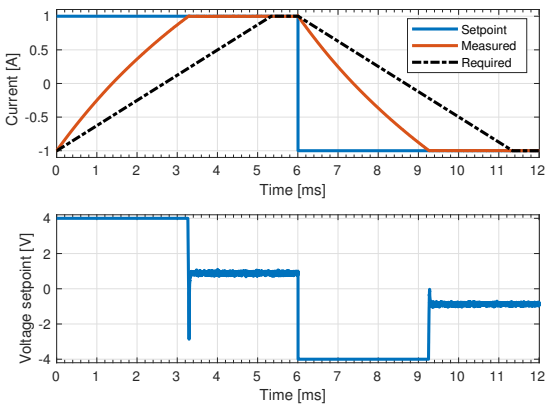

Figure 4: Step response at 100% of full-scale.

The step results presented above refer to extreme cases. Realistic demands for fast variations of the corrector currents should have much lower slew rates. Typical disturbances will be concentrated below 100 Hz, be it sinusoidal (e.g., vibrations, ripple) or ramp (e.g., ID parameter changes).

Noise Spectral Density

NSD has been validated by recording 0.95 s of current data at different DC levels, as depicted in Fig. 5. It shows a slight noise amplification around the closed-loop bandwidth of 13 kHz. The disturbance rejection at lower frequencies mitigates mains ripple and slow current drifts mainly caused by the power amplifiers. It should be noted that, since the current data comes from in-loop measurements, the noise content below the loop banwdwidth will be dominated by the ADC noise floor instead of the measured noise, as shown in the curve measured with amplifier off and current loop open. The overall achieved channel NSD can be roughly considered flat at 200 nA/$\sqrt{\text{Hz}}$ for higher frequencies, while exhibiting $1/f$ behavior with corner frequency around 100 Hz. Such performance exceeds the requirement.

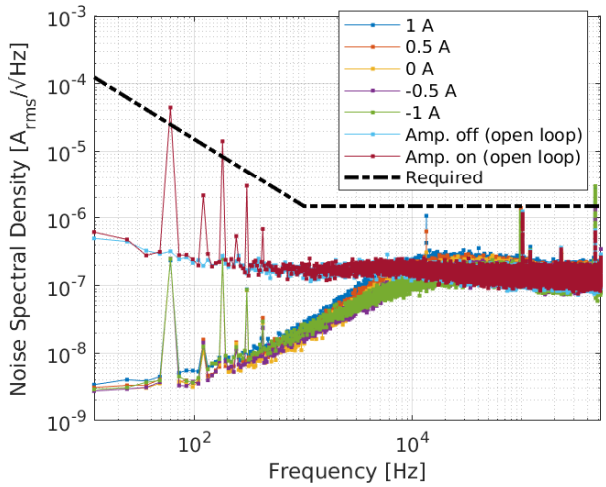

Figure 5: Noise Spectral Density at different DC values.

Power Efficiency

The efficiency of the buck converter for the power amplifiers was measured at 92.5% (V_{in} = 11.8 V, I_{in} = 2.71 A, V_{out} = 3.62 V, I_{out} = 8.17 A), so 29.6 W are effectively usable by the power amplifiers. For 8 channels running up to 1 A each, the power amplifiers can be supplied with 3.7 V for the best performance while respecting the maximum total power draw of 36 W.

CONCLUSION

The prototype validation of the Sirius fast orbit corrector power supply in MicroTCA.4 form factor is ongoing and has satisfied the main design requirements already. The main issue found was the interference of DAC output with the current measurement. Although this effect could be attenuated by delaying the DAC update in relation to the ADC aquisition, possible hardware improvements will be investigated. Further optimization of buck controller and channel-to-channel isolation are also foreseen as continuation of the validation work.

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