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FIRST TESTS OF BEAM POSITION MONITOR ELECTRONICS WITH BUNCH RESOLVING CAPABILITIES

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Abstract

We are reporting on first tests of a beam position monitor using 1 GS/s data streams of signals from a four button pickup. The system digitizes signals of ≈ 2 GHz bandwidth using a choice of sampling frequency that realizes equivalent time sampling. The data is subsequently processed in the Fourier domain to unfold the aliased spectral lines and apply an impulse response correction per channel. After transforming back into time domain, individual bunch signals can be clearly identified and selected for further processing and decimation. The paper will provide detail on the hardware implementation and demonstrate the bunch resolving capabilities, long term stability and beam intensity dependence using beam tests in BESSY-II and synthetic signals.

INTRODUCTION

Digital Beam Position Monitors (BPMs) have become common place in accelerators owing to their good position resolution, flexibility in data rates and their outstanding stability [1–3]. The receiver principle is based on Software Defined Radio, with an Analogue to Digital Converter (ADC) followed by a Digital Down Converter implemented in a Field Programmable Gate Array (FPGA). This receiver realises a Digital Down Converter which picks one spectral line associated with the bunching frequency of the accelerator and achieves high signal to noise ratio by processing gain realised through filtering and decimation.

In many existing implementations, the ADC undersamples the bunched beam signal and uses a narrow band filter in the analogue front end to avoid frequency aliases [4]. As a consequence, parts of the beam spectrum are lost and bunch by bunch information can no longer be reproduced [5]. Time resolution scales inversely to bandwidth, so typical filter bandwidths of 10 MHz will only provide a time resolution of 100 ns.

Recent developments in storage rings introduce bunches on different orbits [6–8]. As a consequence, BPMs able to resolve and select individual bunches for processing are required and these demand a significantly larger signal bandwidth to realise bunch by bunch time resolution.

The new development investigated in this paper continues from ideas presented earlier [9] while extending the acquisition to four parallel channels and increasing the sample rate by factor 14, thus creating a raw data rate more than 50 times larger and reaching 8 GBytes/s per BPM.

INVESTIGATED HARDWARE

Giga-sample speed ADCs with 14-16 bit resolution are available packaged with FPGAs and memory as commercial off the shelf (COTS) products. We selected four products from different manufacturers to cover a range of aspects including ADC type, form factor, AC/DC coupling and FPGA resource usage for our first investigations as listed in Table 1.

For our prototype implementation we used the ability to record large sets of ADC data from all channels at full rate into the on-board RAM. The record set was transferred through a Peripheral Component Interconnect Express (PCIe) connection into the main memory of an adjacent Central Processing Unit (CPU) for further processing and display.

An unexpected behaviour was discovered on the NI-PXIe-5764: When supplied with a signal at 500 MHz with on/off modulation resembling a partially filled ring, the records taken at 1 GS/s showed erroneous samples during the off period (see Fig. 1). The same behaviour was also later found with the FMC231, which uses the same ADC chip. After investigations, both manufacturers related this behaviour to the DC Offset Correction Block in the ADS54J60. This component employs four interleaving ADCs in each channel. The erroneous behaviour has only been observed at input frequencies within 1-2% of a quarter or half the sampling frequency, which is unfortunately the case in our application. As a consequence, we did not perform any further tests with these boards despite the lower Noise Signal Density (NSD) these boards would offer.

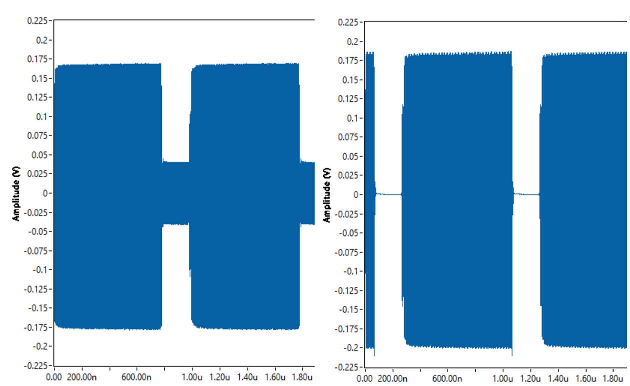

Figure 1: Pulse modulated signal recorded using NI-PXIe-5764: left 500 MHz signal, right 600 MHz signal.

Characterisation Setup

In all further tests reported here, the signal was split four-way using a resistive splitter and short semi-rigid cables connecting to the inputs of the ADC boards. The input to the splitter was then either connected to a signal generator or directly to a button pickup in the BESSY II storage ring. These two signal sources provide complementary features: while the signal generator offers immediate control

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Table 1: Compared ADC/FPGA Boards. Common to All Devices Are Four Channels of 1 GS/s ADC with Internal and External Clock, On-board RAM >1 GByte, Control and Readout Through PCIe

Device	**Teledyne SP Devices ADQ14DC-4C-MTCA**	**Teledyne SP Devices ADQ14AC-4C-PXIE**	**National Instruments PXIe-5764**	**Vadatech FMC231 on AMC525**
ADC chip	2 x AD9680	2 x AD9680	2 x ADS54J60	2 x ADS54J60
ADC coupling	DC	AC	AC	AC
Form factor	MTCA	PXIe	PXIe	MTCA
FPGA	Kintex 7 K325T	Kintex 7 K325T	KU040	Virtex-7 X690T
Full range [V]	1.9	1.9	2.0	1.9
NSD [dBm/Hz]	-142.6	-145.5	-147.3	(not determined)

of frequency and power, the pickup signal features the full spectrum and peak voltages of the final application. No further front-end electronics were employed, the attenuation of the resistive splitter (12 dB) was enough to fit the button signal to the ADC input. For the future, options with programmable broadband attenuators or low pass filters to limit the harmonics in the spectrum are under consideration.

Blocks of 1 M samples spanning a duration of 1 ms were recorded and then analysed for channel amplitudes. The four amplitudes V_A, V_B, V_C, V_D were converted to represent beam positions X, Y using the Δ/Σ approach and a geometric scale factor of $k_{x,y}$=10 mm arbitrarily selected for comparison with other instruments:

$$X = k_x \frac{V_A - V_B - V_C + V_D}{V_A + V_B + V_C + V_D} + X_{\mathrm{off}}$$
$$Y = k_y \frac{V_A + V_B - V_C - V_D}{V_A + V_B + V_C + V_D} + Y_{\mathrm{off}}.$$

This focuses on differential stability of the channels while ignoring common variations caused by the source. No real beam positions were measured in this paper, but deviations between ADC channels are expressed as if they are used as a BPMs. Remaining offsets from fixed channel deviations have been subtracted in all displayed results.

TEMPORAL RESOLUTION

The individual button signals with bunching frequency f_B = 499.66 MHz are recorded with a sampling frequency of $f_S = 2048/1025 \cdot f_B \approx 998.22$ MHz. With this sampling frequency exactly 41 turns in the BESSY II storage ring are acquired using 32,768 samples and following equivalent time sampling principles the repeating fill pattern will be digitised with a time resolution of $\tau = 1/(41 \cdot f_S) \approx 24.4$ ps.

An example of the signal quality achieved using this approach is shown in Fig. 2. A short duration of the fill pattern in the BESSY II storage ring is shown, depicting an isolated single bunch and the beginning of the following bunch train. These records indicate the high level of temporal resolution that can be achieved with 1GS/s operating in this way. The higher bandwidth of the AC coupled board results in sharper pulses with larger amplitudes. However, the particular example also shows issues with ringing following the single

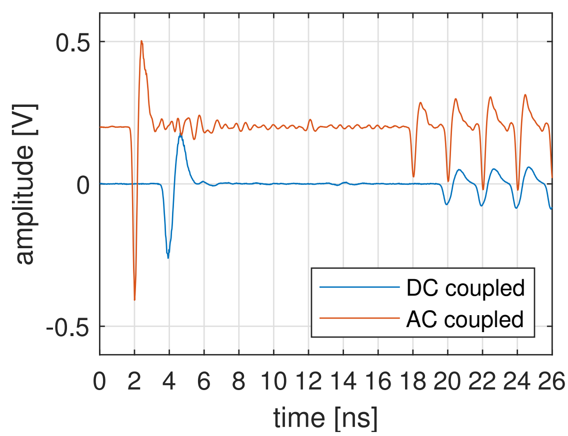

Figure 2: Example of single button pickup signal in BESSY II acquired with the ADQ14 boards and process as equivalent time sampling. The AC signal is offset in time and voltage to improve visibility.

bunch on the AC coupled trace, which we believe might be related to poorer input matching.

Instead of re-ordering samples to create an interpolated time axis, we have employed a procedure where blocks of 32,768 samples are transformed to frequency space using a Fast Fourier Transform (FFT). Due to the repeating nature of the fill pattern, the frequency bins are sharply defined with no leakage. This allows collection of bins at multiples of revolution frequency to assemble a new frequency vector reaching to several GHz, limited only by the analogue bandwidth of the ADC input and coupling, see Fig. 3.

STABILITY AND RESOLUTION

At first we conducted a two week test with a signal generator set to fixed output power and frequency. After converting the amplitudes to position, the standard deviation of 100 successive 1 ms records was found at an average of 300 nm in both planes. Thus a block average filter was applied to reduce the impact of the shot to shot noise in the calculation of medium term stability. The peak to peak stability of resulting 100-point averages over the course of two weeks was 1 m, better than expected given that no means of long term stabilisation like input multiplex switching or pilot tone

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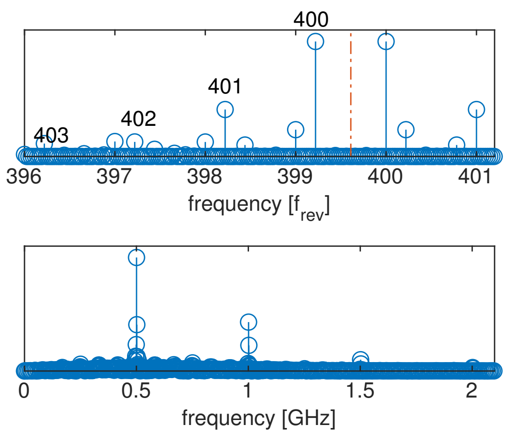

Figure 3: Frequency spectra of single button signal. Top: frequency bins near Nyquist frequency (red), labelled by harmonics of revolution frequency. Bottom: unfolded frequency spectrum clearly showing bunching harmonics at multiples of bunching frequency.

insertion have been employed. Following these encouraging generator test, both boards were connected directly to a button signal. For the period of the test, the beam current was kept in the range 297-299 mA using top-up operation. Consequently, the provided signal power was held within better than 0.06 dB. The results are displayed in Fig. 4 and shows medium term stability within 1 m peak to peak.

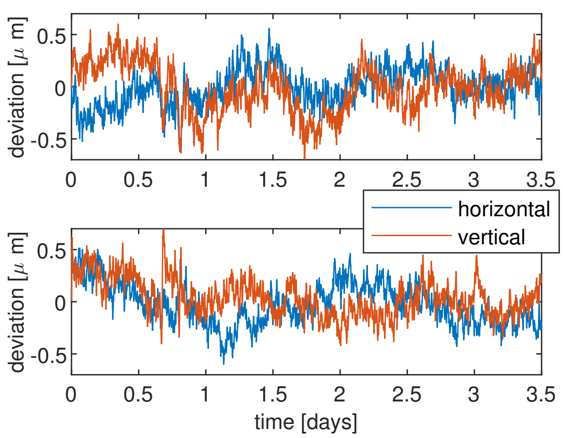

Figure 4: Medium term deviations of calculated position with four way split button pickup signal supplied to inputs of ADQ14. Block averaged over 5 minutes to suppress shot to shot variations. Top: DC coupled, bottom AC coupled.

No clear difference is visible between the AC and DC coupled versions in terms of medium term stability, however on the shot to shot variations of the DC coupled version were found at around 350 nm versus 300 nm for the AC version during this test. The slight increase of these variations in comparison to the signal generator test might be related to the lower signal power from the beam, while the better performance of the AC version can be explained by the slightly lower NSD.

BEAM INTENSITY DEPENDENCE

Another important demand on BPMs is a independence of the position reading from the beam current in the storage ring, of particular importance where operating with decaying beam. The challenge is the variation of signal amplitudes and power over a large range. We evaluated the ADC boards supplied by a signal generator and scanned the power over a 50 dB range. The results in Fig. 5 display reasonable tracking of the four channels, if not as good as other BPMs with multiplex switching and programmable attenuators in the analogue front end [1].

Some test with signal from decaying beam in the storage ring were performed as well, but were limited in dynamic range to less than 10 dB and revealed no different results.

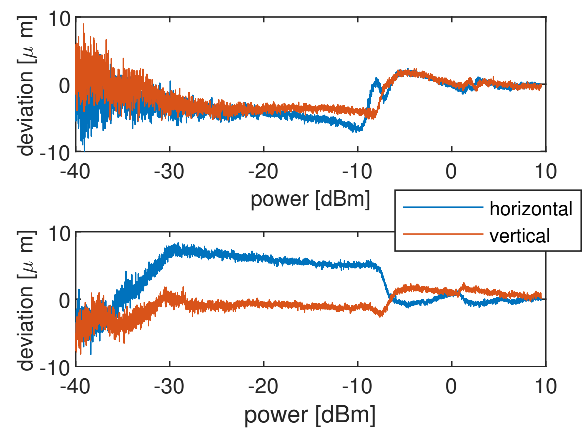

Figure 5: Deviations of calculated position reading as a function of input power per channel with four way split generator signal supplied to inputs of ADQ14. Top: DC coupled, bottom AC coupled.

CONCLUSIONS AND OUTLOOK

In these tests, existing COTS hardware has been evaluated with a perspective to realising BPM electronics with bunch resolving capability. We showed that by digitising the buttons signals directly with individual high speed ADCs the analogue front end can be minimised while achieving excellent resolution and bunch separation. Medium term stability provides satisfactory results, but beam intensity dependence may require further investigations.

The prototype implementation relied on processing in the CPU which is not capable of receiving (due to PCIe on the backplane) or processing (due to limited CPU performance) the whole raw data rate. We will thus move to data processing and decimation in the FPGA as a next step.

We also continue to perform further tests, for example resolution at various data rates, fill pattern dependence, stability at off centre locations, and impact of bunches on different orbits.

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