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TUNED DELAY UNIT FOR A STOCHASTIC COOLING SYSTEM AT NICA COLLIDER

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Abstract

Stochastic cooling is one of the crucial NICA (Nuclotron-based Ion Collider fAcility) subsystems. This system requires fine tuning of the response delay to the kicker, for both longitudinal and transverse stochastic cooling systems. The use of a digital delay line allows to add additional features such as a frequency dependent group velocity correction. To analyse the capabilities of the digital delay unit, a prototype of the device was created and tested. The article presents the characteristics of the prototype, its architecture and principle of operation, test results and estimations for the future developments.

INTRODUCTION

The one of the challenging technologies of the NICA heavy-ion collider project is the stochastic cooling, which is required to suppress the intra-beam scattering effect to increase the luminosity of colliding beams.

The stochastic cooling system is a broadband microwave beam feedback system that reduces the random component of betatron and synchrotron oscillations of the beam particles. The working principle is following: pickup electrodes detect the noise component of the beam current, the signal propagates through the system and applies as opposite force at the kicker. For effective operation, the signal must be properly amplified and time-aligned. This opposite signal statistically dumps down transverse or longitudinal divergent patterns of the beam particles.

The Stochastic System at Nuclotron

The necessity of using stochastic cooling in the constructed NICA collider rises preliminary experimental investigations of the possibilities of the method obligatory. Before the run of NICA, a prototype channel was installed at Nuclotron. In stochastic tests at the Nuclotron, it accelerates protons or C6+ ions up to 3÷4 GeV/n with 1e9-1e10 particles in the beam. It has a circumference of 251 m and a beam revolution frequency of ~1.15 MHz/rev.

The pickup and the kicker are placed on straight sections of the ring, diametrically opposite to each other, so the time of flight of the beam from the pickup to the kicker is about 400 ns, and the transit time of the RF signal through the feeder cable is about 270 ns. This system uses a frequency band from 2 up to 4 GHz, -60 dBm signal power from the pickup and 2-stage amplifier, and 60 W maximum output power [1].

At the first stage of research, it was decided to implement stochastic cooling in the longitudinal phase space by mean of the notch filter method, as it is the least critical to the quality of the accelerator tuning. A simplified diagram of a stochastic cooling system is shown in Fig. 1 [2].

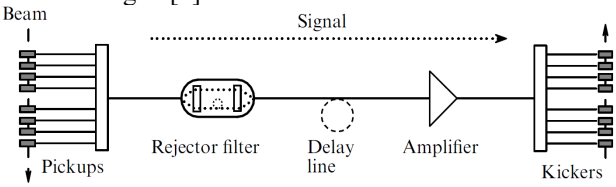

Figure 1: The stochastic cooling system at Nuclotron.

The stochastic system consists of a pickup with preamplifiers, a block of switches, a notch filter, a variable delay and diagnostic devices to maintain different modes of operation, a main amplifier and a kicker. For longitudinal cooling, the pickup is designed to measure the longitudinal beam profile by summing signals from all electrodes into one [3].

The signal to the kicker is generated using a notch filter [4]. Its frequency response is a series of evenly spaced minima in the transmission band, and the phase is inverted at each minimum. If the filter minima exactly coincide with the harmonics of the beam inversion frequency, the signal after the filter becomes proportional to the deviation of the particle in frequency and the beam will be cooled.

Within the filter, the pickup signal converted in optical form, is divided in two legs, in one of which the signal is adjustedly delayed by the beam repetition period, and in both legs the signal powers is adjusted by attenuators. As a result, if the delay time and amplitudes in the notch filter, as well as the delay in the optical delay line are adjusted correctly, the correction signal does not affect equilibrium particles, but accelerates slow particles and slows down fast ones, i.e., decreases the momentum spread of the longitudinal component.

Within the framework of this experiment, the momentum cooling of a coasting beam was obtained [5]. The RMS momentum spread was reduced by approximately a factor of 2.2 within 480 s.

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THE DIGITAL DELAY UNIT

A uniform group delay of the radiofrequency feedback signal is essential for effective stochastic cooling. There are many distorting factors in a purely analog system such as imperfect characteristics of the pickup, filters, delay line and kicker. Phase response correction can be implemented using digital signal processing circuitry. In addition, this circuit can be used to tune the delay and, with some additional feedback, to implement a notch filter.

For testing these tasks, it was decided to implement a digital delay unit, which can replace the optical delay line, and on which the phase response correction can be implemented.

For this purpose, a digital delay unit was developed. In the first test mode, that unit can delay up to two -60 dBm 2-4 GHz signals from the pickup by 108-135 ns with ~52 ps step.

The Digital Delay Unit Description

The digital delay unit of radiofrequency signals should contain: analog-to digital converters (ADC); digital controller with interface for remote control, delaying digitized signals; and digital-to analog converters (DAC). -60 dBm signals from the pickup should be normalized to the ADC input range.

For the 2÷4 GHz frequency range we selected ADC and DAC with maximum acceptable sample rates and minimum propagation delay: ADC07D1520 with 3 GSPS, and DAC5670 with 2.4 GSPS. According to Nyquist's theorem, the maximum frequency range of input signals cannot exceed half the sampling rate. So, we need to shift and reduce the input frequency range in front of the ADC. This is possible using quadrature demodulators and modulators, which converts one signal with 2÷4 GHz range to two signals with 0÷1 GHz before the ADCs, and do an inverse conversion after the DACs by mixing the delayed signal with 2 heterodyne signals, shifted relative to each other on 90 degrees.

So, a simplified digital delay block diagram is shown in Fig. 2.

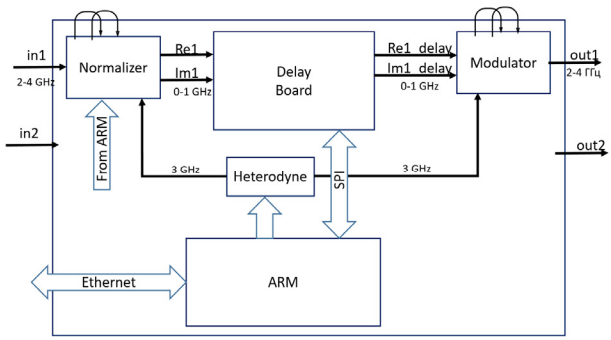

Figure 2: Digital Delay Unit.

It consists of: a signal normalizer, which contains 3-stage 60 dB wide range amplifier, an attenuator of 0÷31 dB, additional 20 dB amplifier and a downconverter; a digital delay module with two 2-channel ADCs, an FPGA, four DACs and a HMC7044 dual-loop clock frequency generator. The digital delay board is shown in Fig. 3.

Additional infrastructure modules of the unit are: LMX2572-based 2-channel 3 GHz heterodyne generator; 12-channel power supply; and a microcontroller board Atmel SAM E70 Xplayned [6], based on the ATSAME70Q21 ARM Cortex 7 microcontroller; this board is used as an interface and configuration module of the unit.

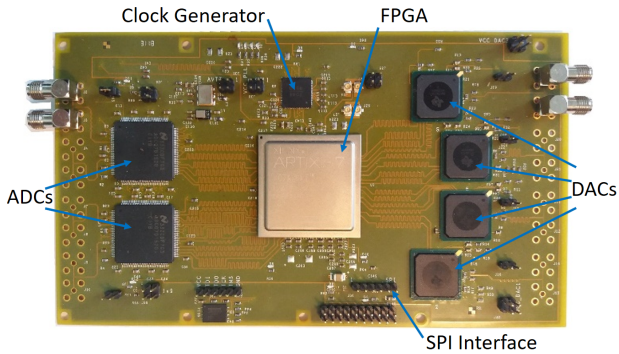

Figure 3: Digital Delay Board.

The Delay Prototype Unit Software Configuration

For the prototype, the operating mode with the maximum possible bandwidth of the RF signal is selected. In this configuration, ADC works in Dual Edge Sampling mode with a clock frequency 1.2 GHz and a sampling rate 2.4 GSPS, and the DAC works at a 2.4 GHz clock rate. In this mode, one ADC can digitize only one RF signal, which requires the use of both ADCs for one RF signal from the pickup, which is enough for longitudinal stochastic cooling.

A simplified block diagram of FPGA in prototype mode is shown in Fig. 4.

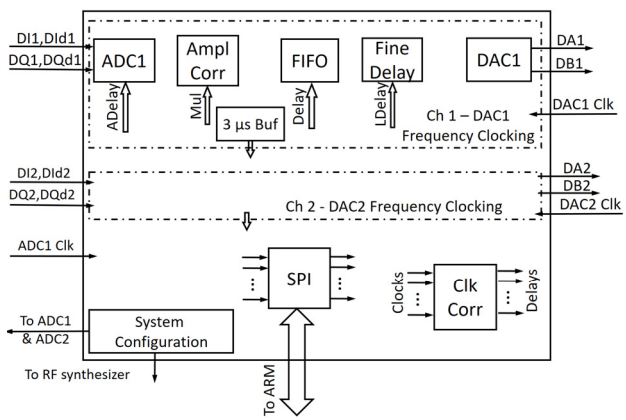

Figure 4: FPGA Firmware.

In this mode, each ADC transmits a digitized signal over four 7-bit data buses clocked at 300 MHz. The digitized signal is processed in the FPGA by the following sequence of modules. The input ADC modules in the FPGA receive the digitized data on both edges of the 300 MHz clock signal, packing them into an 8x7-bit and then into 16x7 bit register with data rate reduced down to

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150 MSPS. This data is stored in a 3 μs buffer and could be visualized by the connected PC. The next module normalizes the signal amplitudes.

Then, after the backward serialization, the data goes to the two-stage delay module. The 1st stage of the delay module delays data in 1/300 MHz step and is implemented on the basis of a dual-port memory. The 2nd stage of the delay module uses 2 methods of signal delay: a word shift within the 8x7 bit data bus allows to change the signal delay in 2.4 GHz steps; linear data interpolation between adjacent ADC readings in 1/8 steps allows data delay to be changed in 1/(300 MHz x8x8) ~ 52 ps steps. Then the data is output to the interface modules for external DACs via the 8x7 bit bus. The interface modules provide data to the DACs over two 14-bit buses at 600 MHz, allowing the DACs to update the amplitude of output signal at 2.4 GHz rate.

A separate task in the FPGA module is to automatically adjust the phase of clock signals to various modules involved in the wiring of the digitized ADC signals. The original clock signal was a 600 MHz clock from the DAC chip. The procedure for measuring and automatically adjusting the phase of signals is similar to the algorithm used in the Digital Dual Mixer Time Difference [7], which is used, for example, in the White Rabbit synchronization system [8].

TEST RESULTS

Test sequence produced with PC-based control program. That include: the delay of the output sinusoidal signal with a constant frequency, the amplitude-frequency, phase-frequency, and step response of the delay line, the group delay of the module, as well as the spectra of the sinusoidal signal from an external generator were measured. Final on-table test result is shown on Fig. 5. It optimizes worked signal amplitude related to a certain set of intermodulation spectral components on full frequency range.

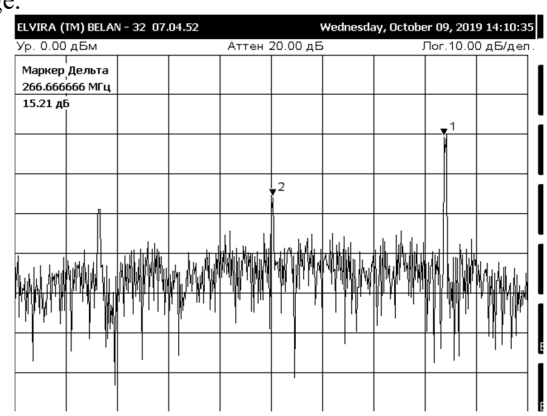

Figure 5: Worked signal amplitude tuning.

FUTURE DEVELOPMENTS

The results of testing the original design of pickups and kickers from FZJ at the Nuclotron showed that it does not fully meet the requirements of the NICA accelerator [9]. First, the use of this pickup will not allow obtaining the required pressure of 1e-11 Torr, since there are many small elements in the pickup. In addition, the maximum frequency response measured is 2.4 GHz rather than 3 GHz. Therefore, it was decided to use a ceramic vacuum chamber with external electrodes.

The addition of a ceramic vacuum chamber has shifted the pickup bandwidth to 1÷2 GHz, which can be changed to required 2÷4 GHz [10], but currently the set of delay units should work with these frequency ranges: 0.70-1.05 GHz, 1.27-1.91 GHz, 2.13-3.20 GHz.

This greatly simplifies the circuits of the quadrature modules of the amplifier-normalizer and modulator, firmware of the FPGA and allows us to reduce the minimum signal delay in the delay unit, since now the ADC and DAC can directly measure these frequency ranges, therefore the modules before the ADC and after the DAC must only shift the frequency ranges, and do not require dividing one analog signal into two digital ones.

In any case, the digital implementation of the delay module allows us to add a phase response correction. Basically, the constant phase response of an RF line can be corrected by measuring the phase response of the delay line and generating a phase-correcting FIR or IIR filter. Later, the phase response can be adjusted automatically.

Reducing the minimum propagation delay through the digital delay unit is a crucial task for improving the phase response correction, since a finer correction filter within an FPGA requires a higher signal delay. The minimum signal delay within the prototype delay unit is ~108 ns, which is almost unacceptable for phase response correction.

The main parts of signal delay are conversion time in ADCs and DACs, and signal delay within FPGA. The minimum delay for low-resolution ADCs is ~15 ns. Other high-rate ADCs demonstrate much longer conversion due to internal conveyer structure, in particular this is the case for system-on-a-chip solutions such as Xilinx Zynq UltraScale+ RFSoC series. On the other hand, it is possible to sufficiently minimize the FPGA delay from ~90 ns for prototype unit down to ~50 ns by simplifying FPGA design in accordance with the new requirements for the delay unit, and even more by fine-tuning the FPGA design.

CONCLUSION

A prototype of a digital delay unit for the NICA heavy-ion Collider stochastic cooling system was developed and tested. In the first test mode, that unit can delay up to two -60 dBm 2-4GHz signals from the pickup by 108-135 ns with ~52ps step. These possibilities should be acceptable for the for longitudinal stochastic cooling system Digital processing circuit can be used for phase response correction, which is crucial for a uniform group delay of the radiofrequency feedback signal. Reducing the minimum propagation delay through the digital delay unit is a crucial task for improving the phase response correction.

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