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A RECENT UPGRADE ON PHASE DRIFT COMPENSATION SYSTEM FOR A STABLE BEAM INJECTION AT J-PARC LINAC

E. Cicek*, Z. Fang, Y. Fukui, K. Futatsukawa, KEK, Ibaraki, Japan
T. Hirane, S. Shinozaki, JAEA/J-PARC, Tokai-mura, Japan
Y. Sato, Nippon Advanced Technology Co., Ltd., Tokai, Japan

Abstract

J-PARC linac, consisting of 324 MHz and 972 MHz acceleration sections, delivers H^- beam to the rapid cycling synchrotron (RCS). The drift in the beam injection momentum from linac to RCS was measured to be highly dependent on the humidity at the klystron gallery. Also, changes in both temperature and humidity strongly affect the rf field phase controlled within the digital feedback (DFB) system. To cope with this, a unique phase drift compensation system, namely the phase drift monitor (PDM) system, is implemented in the MEBT2B1 station as the first step at the linac. However, the compensation of the drift correction could not be achieved directly since two different frequencies were used. The new PDM, which adapts the direct sampling method using the Radio Frequency System-on-Chip (RFSoC), will pave the way to ensure rf phase stability at all stations simultaneously. Here we present the effects of temperature and humidity on the rf field phase, along with performance and preliminary test results concerning the phase drift compensation.

INTRODUCTION

The J-PARC (Japan Proton Accelerator Research Complex) linac consists of a 50 keV negative hydrogen (H^-) ion source, a 3 MeV radio-frequency quadrupole (RFQ), a 50 MeV drift-tube linac (DTL), a 191 MeV separated-type DTL (SDTL), and a 400 MeV annular-coupled-structure (ACS) [1]. Produced H^- beams are accelerated by 324 MHz and 972 MHz accelerating rf structures and delivered to 3 GeV RCS with injection energy of 400 MeV.

The drift in the beam injection momentum from linac to RCS is highly dependent on the humidity, and a momentum spread of less than $\pm 0.1\%$ is required at the injection point of the RCS following the linac. Thus, achieving long-term stable beam injection requires stabilized rf field phase at all stations. Currently, phase drift in the 324 MHz and 972 MHz rf accelerating frequencies generated at each LLRF station is compensated by dedicated cavity phase monitors. Each rf signal is down-converted to the intermediate frequency (IF) signal of 12 MHz. Subsequently, the IF signal is measured by 48 MHz sampling frequency in the FPGA, IQ components are obtained, and the amplitude and phase differences are calculated [2]. However, the phase drift compensation for each frequency is implemented independently. To this end, to evaluate drift in two different rf frequencies directly and maintain a long-term stable beam injection, a unique phase drift compensation system, so-called PDM, is built and tested in the linac. With this system, we aim to reduce beam losses; thus, enhance the stable operation of the accelerators. Several pick-up rf signals from the SDTL15A, SDTL15B, SDTL16A, and SDTL16B cavities, operating at 324 MHz, are connected to the first four analog-to-digital converters (ADC) channels ADC00~03. On the other hand, MEBT2B1, MEBT2B2, and ACS1 cavities that operate at 972 MHz are connected to ADC04~06 channels (Fig. 1). Constant temperature and humidity are provided for LLRF control racks of the SDTL16A, SDTL16B, and MEBT2B1 stations and also the PDM system. Hence, the rf field phase of these cavities, which will be assigned as reference phases for the other cavities, is fixed. Possible phase differences between these and the other cavities are monitored and compensated in the DFB system. The performance evaluation of the PDM system will be mentioned throughout this paper.

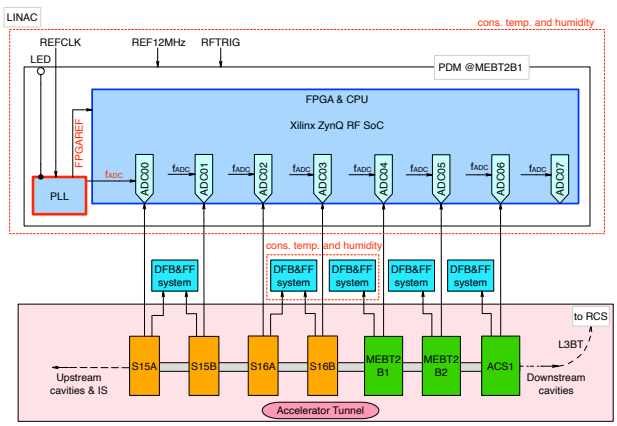

Figure 1: Block diagram of the phase drift compensation system to be implemented in linac.

PHASE DRIFT MONITOR

The PDM system is implemented in a Zynq UltraScale+ RFSoC ZCU111 evaluation board manufactured by Xilinx [3]. The board contains eight 12-bit Xilinx RFSoC's built-in ADCs supporting a high-speed sample rate of 4.096GSPS and an input bandwidth of up to 4 GHz; also eight 14-bit (6.554GSPS) RFSoC DACs, which are key features of the device compared to that of traditional counterparts. The configuration of the PDM system with signal processing to be implemented is shown in Fig. 2. Note that Fig. 2 represents the system implementation for two adjacent ADCs. It is essential to measure rf signals in linac having two different operating frequencies to eliminate the

* ecicek@post.kek.jp

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effects of temperature and humidity on the beam injection momentum. Therefore, we adopted a direct sampling method for phase detection [4, 5]. In this technique, the 324 MHz and 972 MHz input rf signals from cavities are directly digitized by ADCs. Then, IQ components are obtained by the DDC. The 3888 MHz ADC sampling frequency for A/D conversion, is generated by the 972 MHz external REFCLK multiplied by four in phase-locked-loop (PLL). The initial phase of the IQ conversion is decided by the rising edge of the 12 MHz input as a reference. The REF12MHz signal, directed from the 12 MHz delay module, is employed to ensure phase reproducibility. Subsequently, amplitude and phase information of the IQ-converted values are adjusted by multiplying with the rotation coefficients (A, B, C).

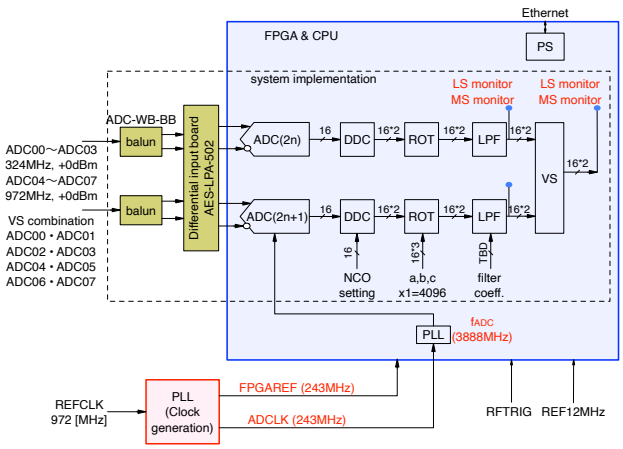

Figure 2: The functional block diagram of the PDM system. DDC, ROT, LPF, VS, and PS indicate digital down converter, IQ rotation, low-pass filter, vector sum, and processing system, respectively, whereas REFCLK, REF12MHz, RFTRIG, ADCLK, and FPGAREF indicate reference 972 MHz clock, reference 12 MHz signal, rf trigger, ADC clock, and FPGA reference clock, respectively.

A cavity-based digital IIR filter (LPF) is implemented to the baseband IQ values to remove high-frequency noise and to suppress the parasitic modes in the cavities of linac [6] and hence to improve the phase stability. The output of the LPF is monitored by a low-speed monitor (point data) and a medium-speed monitor (waveform data). As a final step, I/Q mean values of the ADC(2n) and ADC(2n+1) combination are also monitored after the VS process.

The board is also embedded with an input/output controller (IOC) application based on Experimental Physics and Industrial Control System (EPICS). The EPICS IOC is built and runs on the board to set, read back, and monitor the control parameters via Ethernet.

PERFORMANCE EVALUATION

The performance of the PDM system has been evaluated with the test setup seen in Fig. 3. The first four ADC channels, ADC00~03, and the other channels, ADC04~07, are reserved for 324 MHz and 972 MHz frequencies, at which the accelerators in the J-PARC linac are operated, respectively. The 324 MHz signals from SG2 are divided by four: each identical signal is directed to the first four ADCs on the PDM. The 972 MHz signals generated by the SG1 are first split in two: one is utilized for the REFCLK input, and the other one is directed to the 4-way divider to realize power on ADC04~07. An FG is also employed to generate signals for RFTRIG and REF12MHz. The SG1, SG2, and FG are synchronized to each other by 10 MHz signals.

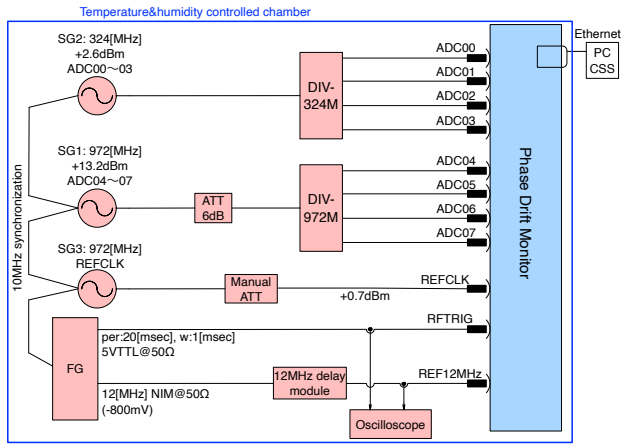

Figure 3: Schematic diagram of the PDM test setup. SG1&SG2, FG, DIV324M&DIV972M, and ATT indicate signal generators, function generator, 4-way dividers, and attenuator, respectively.

Amplitude and Phase Stabilities

Amplitude stability (peak-to-peak) for ADC00 (and ADC04) at CW mode has been measured as ±1.18% (±1.16%), ±0.86% (±0.87%), and ±0.63% (±0.67%) for the ADC amplitude of 2000, 3000, and 4000, respectively. The amplitude stability decreases with the increase of ADC amplitude; hence white noise is dominant. Also, the peak-to-peak phase stability of ADC00 (and ADC04) channels was measured as ±1.21 deg. (±3.14 deg.), ±1.04 deg. (±2.23 deg.), and ±1.42 deg. (±2.86 deg.) again for the ADC amplitude of 2000, 3000, and 4000, respectively. There is a noise of about 4 kHz, observed not in amplitude but only dominant in both ADC00 and ADC04 phase data.

Crosstalk

The crosstalk level for ADC channels has been evaluated when rf power is realized on a particular ADC channel. Thus, if 324 MHz and 972 MHz rf signals with specific power values are applied on ADC00~03 and ADC04~07 channels, respectively, the crosstalk level was estimated to be less than -62 dB in each channel. On the other hand, the crosstalk level for the ADC05 channel is slightly less than that of other ADC channels (Fig. 4).

Moreover, we have also observed crosstalk from REFCLK to the ADC channels. All the ADC channels are terminated by 50 Ω, and power is only realized on the REFCLK (+2.5 dBm). There is a noise at 40.5 MHz only on

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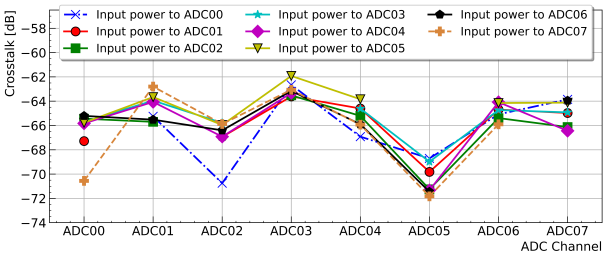

Figure 4: Crosstalk level in the PDM board. Note that the results for the ADC channels are displayed except for the channel in which rf power is applied.

ADC00~03 channels; however, no 40.5 MHz noise on ADC04~07 channels from the FFT calculated for each ADC channel. ADC04~07 channels have a magnitude of about ~3 at 0 Hz (Fig. 5). On the other hand, the magnitude of ADC00~03 is ~3 at 40.5 MHz. Considering the REFCLK frequency of 972 MHz, in the DDC of ADC00~03, a signal is generated (972 MHz − 324 MHz). Therefore, this signal takes on the alias of a different low-frequency component of 40.5 MHz at a sampling frequency of 121.5 MHz.

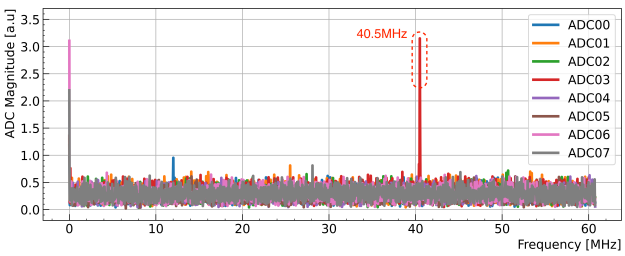

Figure 5: Crosstalk from REFCLK to the ADC channels.

Temperature and Humidity Dependence

PDM was placed in a temperature and humidity-controlled chamber to evaluate the effects of temperature and humidity on the rf phase for ADC04~07 channels.

First, the temperature has been changed from 23 °C to 31 °C with a 2 °C step, and back to 23 °C at a humidity of 65% in the chamber. The system was kept constant at each temperature step applied for 3 hours. The drift in phase per 1 °C was 0.75 deg. (Fig. 6-top). Then, the system was kept at a temperature of 27 °C, and humidity was changed from 15% to 65% at a ramping rate of 25% / 24 hours. At this stage, the phase drifted by about 0.45 deg. per each humidity changing step (Fig. 6-bottom). The phase variation range is about 0.1 deg. in each step. Thus, the PDM can be used in the LLRF system since it will be placed in a temperature and humidity-controlled chamber.

CONCLUSIONS AND FUTURE WORK

The source of 4 kHz noise caused by the A/D clock jitter is most likely due to the power supply on the board or, with a lower probability, the ethernet cable. Further studies should be conducted to get rid of this noise. Moreover, the crosstalk level for the ADC channels was evaluated to be less than -62 dB, and the source of 40.5 MHz noise is crosstalk

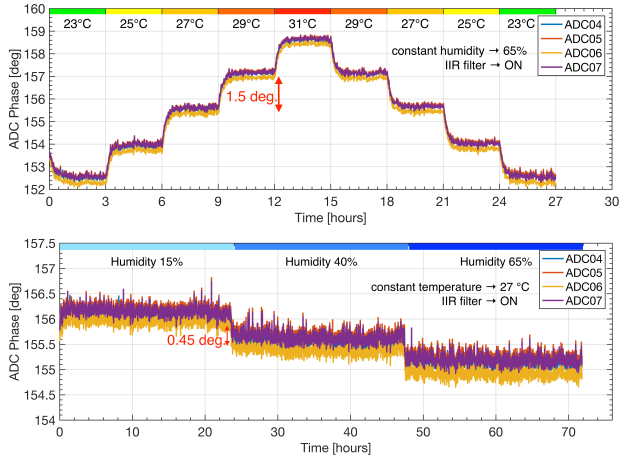

Figure 6: The effects of temperature (top) and humidity (bottom) on the rf phase for ADC04~07 channels.

from the REFCLK to the ADC channels. Furthermore, the study regarding temperature and humidity effects on the rf phase for 972 MHz channels has been completed. However, a digital filter will be employed to suppress fluctuations observed in the rf phases seen in temperature and humidity data. The study concerning the phase drift for 324 MHz channels and the phase difference between 324 MHz and 972 MHz channels will be conducted.

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