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SPALLATION NEUTRON SOURCE PROTON POWER UPGRADE LOW-LEVEL RF CONTROL SYSTEM DEVELOPMENT*

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Abstract

The Proton Power Upgrade (PPU) Project is approved for the Spallation Neutron Source at Oak Ridge National Laboratory and will double the proton beam power capability from 1.4 MW to 2.8 MW with 2 MW beam power available to the first target station. A second target station is planned and will utilize the remaining beam power in the future. The proton power increase will be supported with the addition of twenty-eight new superconducting cavities powered by 700 kW peak power klystrons to increase beam energy while increases to the beam current will be done with a combination of existing RF margin, and DTL HPRF upgrades. The original low-level RF control system has proven to be reliable over the past 15 years of operations, but obsolescence issues mandate a replacement system be developed for the PPU project. The replacement system is realized in a µTCA.4 platform using a combination of commercial-off the-shelf boards and custom hardware to support the requirements of PPU. This paper presents the prototype hardware, firmware, and software development activities along with preliminary testing results of the new system.

INTRODUCTION

The existing digital low-level RF (LLRF) control system has been in operation since 2006 [1] and continues to meet the operational requirements for the Spallation Neutron Source (SNS). As with most fifteen-year-old electronics, obsolescence has mandated that a new control system be developed to support the 28 new superconducting cavities required for the Proton Power Upgrade (PPU) project. One of the main objectives for the new system is to maintain a similar look and feel as the existing system to minimize the learning curve for the new system. This is important because our linear accelerator (Linac) will have a mix of new and old systems until the Second Target Station (STS) project is completed. Once the STS is constructed, all LLRF systems will be upgraded to the new MicroTCA.4 – based equipment. With this upgrade in mind, we designed the new hardware to be easily retrofitted into the original LLRF equipment racks and will reuse portions of the existing system to minimize costs associated with the upgrade.

With 15 years of operational experience, we have discovered several shortcomings in the diagnostics for the existing system. This upgrade has allowed us to incorporate the lessons learned. In the following sections, the various subsystems of the new LLRF system are introduced in detail, along with initial test results from both the benchtop and in-situ Linac operational testing are presented.

LLRF PLATFORM

The existing SNS LLRF system is implemented utilizing the VME extensions for instrumentation (VXI) open standard platform and has been robust over the past 15 years of operation. There are, however, significant processing limitations due to the backplane speed. To solve this limitation, MicroTCA.4 was chosen for the new LLRF platform. This platform was utilized at SNS for the successful implementation of the Ring LLRF systems in 2018 and is becoming widely adopted at other institutions globally. Each SNS MicroTCA.4 crate will support up to two LLRF control systems.

For the PPU LLRF implementation, the VadaTech VT811 12 slot MicroTCA.4 crate along with the UTC002 MicroTCA Carrier Hub (MCH) was chosen (Fig. 1). The UTC002 MCH supports Peripheral Component Interconnect express (PCIe) Gen 3 communication that supports a bit rate of 8 GT/s. This is significantly faster than the expected data rates for our LLRF control system. The addition of intelligent platform management interface (IPMI) in the system allows for enhanced monitoring of board health which we expect will result in improvements to system availability.

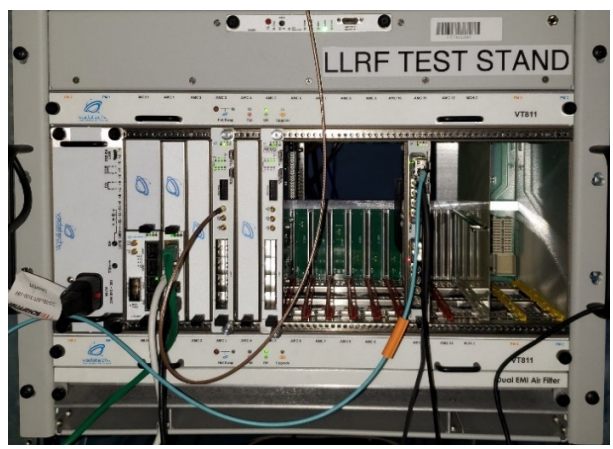

Figure 1: New LLRF platform.

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FIELD CONTROL

The new field control module is architecturally similar to the original system in that it fundamentally realizes a proportional-integral (PI) feedback controller along with adaptive feedforward (AFF) to support cavity filling and beam-loading [1]. The overall regulation requirements for SNS are 1% amplitude, 1° phase, which is significantly relaxed compared to other accelerators. We routinely regulate at 0.5% and 0.5° and expect to achieve better than this level of control on the new system. The system supports up to six inputs to the field control module (FCM-II) as shown in Fig. 2. The primary control inputs are the RF reference, cavity field, cavity forward, and cavity reflected signals. The additional two inputs are for a beam signal and a spare channel to allow for future expansion.

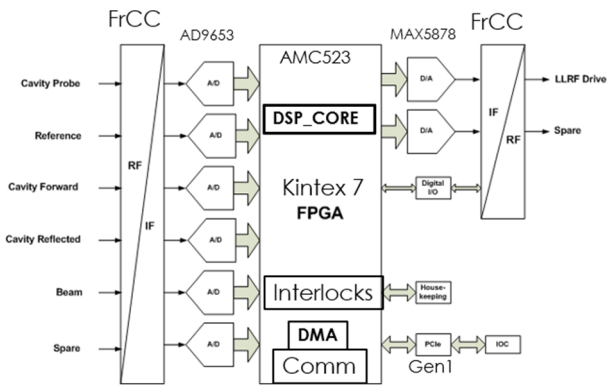

Figure 2: Field control block diagram.

Because we are doing an upgrade to our system but retaining the existing reference and local oscillator (LO) distribution [2], we needed to maintain the 50 MHz intermediate frequency (IF). Due to this limitation, a 12/5 non-I/Q sampling scheme for the analog to digital converters (ADC) was selected. This has provided improved measurement precision by avoiding spectral aliasing [3] and improved the digital signal processing (DSP) pipeline delay due to the increased 120 MHz sampling frequency.

The FCM-II is implemented using a combination of a commercial off-the-shelf (COTS) advanced mezzanine card (AMC) that provides the field programmable gate array (FPGA) (VadaTech AMC523) and a custom rear transition module (RTM). The custom RTM contains two quad ADC integrated circuits (IC) with signal conditioning front ends for a total of 8 ADC inputs. The RTM also provides the 50 MHz intermediate frequency (IF) drive and digital input/output (I/O) interlocks to interface with the remaining hardware.

Field Control DSP Core

The DSP core was upgraded to take advantage of the newer FPGA capabilities while maintaining the overall flow. A description of the original implementation can be found in [4]. The primary changes to the DSP are the additions of the digital down converter (DDC) and digital up converter (DUC) that are now required for non-I/Q sampling. The DSP block diagram is shown in Fig. 3. The details of the PI loop are provided in [4].

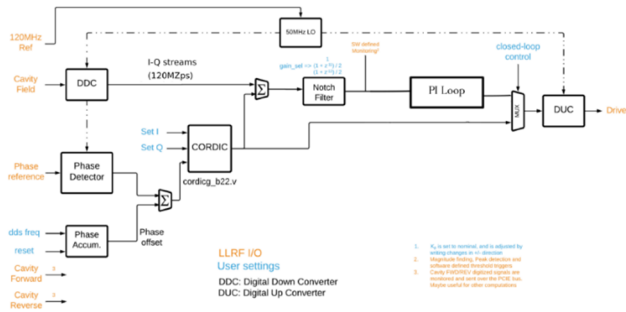

Figure 3: DSP core.

HIGH-POWER PROTECTION

The LLRF system utilizes a combination of a field control module and a high-power protection module (HPM-II) for each cavity control system. The high-power protection module detects faults in the high-power distribution system and interfaces with the field control module and the machine protection system (MPS) to provide for fast shutdown of the RF drive [5]. The HPM-II is implemented using a combination of the AMC523 card and a custom RTM. The custom RTM module is a stacked card that occupies two slots in the MicroTCA.4 crate. The additional space is required to support the I/O for the system (see Fig. 4).

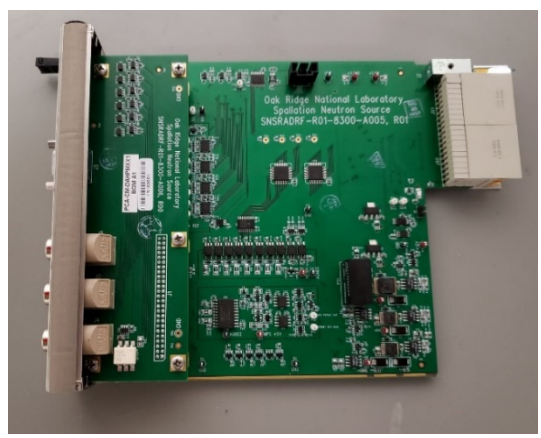

Figure 4: High-power protection module.

RF signals are quickly detected utilizing logarithmic amplifiers (ADL5513) and digitized with 16-bit ADCs providing for a 400-nanosecond sampling period. The detected RF is calibrated and converted into user friendly units that are displayed via Experimental Physics and Industrial Control System (EPICS) screens. The HPM-II provides input for up to 7 RF channels, 1 baseband channel (electron probe), 8 arc detectors, and 5 digital I/O. The RF channel data will be synchronized with the FCM-II data to provide post fault system troubleshooting. Any raw signal can be made available on the front panel of the HPM-II via two 32 to 1 multiplexers.

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FREQUECY CONVERSION CHASSIS

The frequency conversion chassis (FrCC) replaces the down converter chassis on the existing SNS systems and locates all temperature sensitive RF electronics into this thermally compensated chassis. This was done in response to a minor temperature drift that was discovered in the original LLRF control system [6]. As seen in Fig. 5, the down converter (left board), up converter (lower right board), and LO distribution boards are mounted on an 8 mm thick aluminium plate that is maintained at 100° Fahrenheit (+/- 0.1°) to minimize the possibility of drifts.

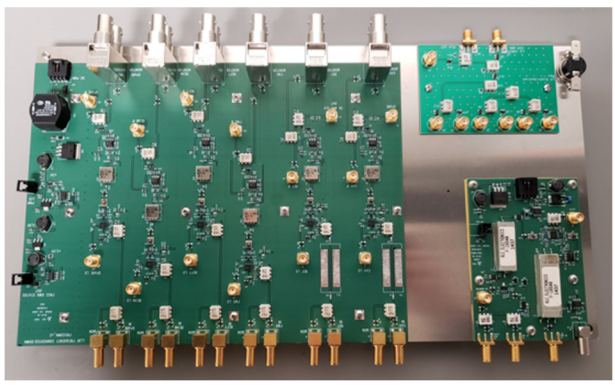

Figure 5: FrCC temperature plate with boards.

For the redesign of the system, active up and down conversion mixers were selected. This reduced the LO power level required and improved the LO to RF and LO to IF isolation numbers. All tested units are measuring better than -70 dBm for LO isolation. Crosstalk numbers also exceed our requirements of -65 dBc with all channels measuring better than -80 dBc.

When the up converter was redesigned, additional output drive capability was added to compensate for occasional low signal gain on the solid-state driver amplifiers for the klystrons. This will provide additional margin for the RF drive signal to help improve availability. Figure 6 is the spectrum of the 805 MHz output signal from the up converter at full power (+17 dBm), all sidebands are supressed past -65 dBm for the required 5 MHz span.

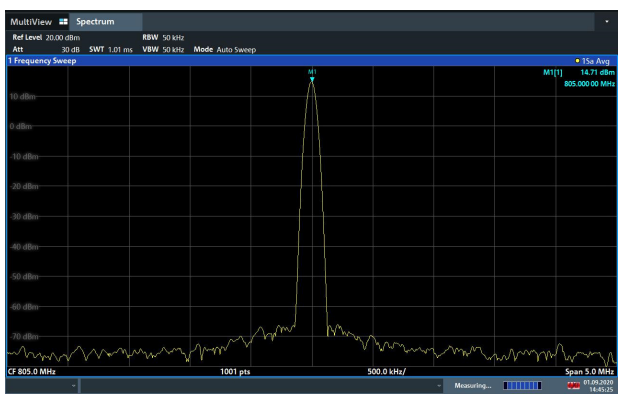

Figure 6: Up converter output – 805 MHz, 5 MHz span.

TESTING

Significant tests of the LLRF system have been completed with over 3000 hours of testing on the field control functions. Standalone integrated bench testing of the FCM-II, FrCC, and HPM-II are ongoing with over 1 year of testing completed. This has allowed the full testing of all hardware interfaces.

Both the original and redesigned LLRF control systems are installed in the equipment rack for the SNS cavity SCL23D, this allows for either system to drive the cavity with only minor cable changes. This has provided opportunities for successful open and closed loop tests with a superconducting cavity during periods of accelerator study time (Fig. 7). With both systems installed, either the original or redesigned system can witness the operation of the other system. On our latest test of the system, we demonstrated 1 Hz beam through the accelerator. While there is still significant integration testing to complete, the initial results are promising.

Figure 7: In-situ Linac testing – closed loop operation.

CONCLUSION

The PPU LLRF control system redesign is complete and the use of COTS hardware whenever possible has significantly shortened hardware development time. Lessons learned over fifteen years of operations have been incorporated in the design to improve operability. Maintaining the look and feel of the operating screens will minimize the learning curve for the operations staff. Initial testing has successfully demonstrated open and closed loop operation with a superconducting cavity. Further beam loaded tests are planned this summer and PPU installation is scheduled for FY 2022.

REFERENCES

[1] H. Ma *et al.*, "SNS Low-Level RF Control System: Design and Performance", in *Proc. 21st Particle Accelerator Conference (PAC'05)*, Knoxville, TN, USA, May 2005, paper WPAT060, pp. 3479-3481.

[2] M. Piller *et al.*, "The Spallation Neutron Source RF Reference System", in *Proc. 21st Particle Accelerator Conf. (PAC'05)*, Knoxville, TN, USA, May 2005, paper WPAT062, pp. 3573-3575.

ISBN: 978-3-95450-214-1 ISSN: 2673-5490 doi:10.18429/JACoW-IPAC2021-WEPAB299

[3] L. Doolittle, M. S. Champion, and H. Ma., "Digital Low-Level RF Control Using Non-IQ Sampling", In *Proc. 23rd Linear Accelerator Conf. (LINAC'06)*, Knoxville, TN, USA, Aug. 2006, paper THP004, pp. 568-570.

[4] H. Ma *et al.,* "Low-Level RF Control of Spallation Neutron Source: System and Characterization", *Physical Review Special Topics – Accelerator and Beams*, vol. 9, p. 032001, 2006. doi:10.1103/PhysRevSTAB.9.032001

[5] M. Crofford, M. Champion, K-U Kasemir, H. Ma, and M. F. Piller, "Operational experience with the Spallation Neutron Source High Power Protection Module", in *Proc. 21st Particle Accelerator Conf. (IPAC'05)*, Knoxville, TN, USA, May 2005, paper WPAT058, pp. 3411-3413

[6] M. Crofford, J. A. Ball, T. L. Davidson, T. W. Hardek, S. W. Lee, and M. F. Piller, "Spallation Neutron Source LLRF Temperature Dependence and Solution", in *Proc. 25th Linear Accelerator Conf. (LINAC'10)*, Tsukaba, Japan, Sept. 2010, paper MOP088, pp. 259-261.