ISBN: 978-3-95450-214-1 ISSN: 2673-5490 doi:10.18429/JACoW-IPAC2021-WEPAB321

ALS-U INSTRUMENTATION OVERVIEW*

J. Weber†, J. Bell, M. Chin, S. DeSantis, R. Gunion, S. Murthy, E. Norum, G. Portmann, C. Serrano
Lawrence Berkeley National Laboratory, Berkeley, CA, USA
W. Lewis, Osprey DCS, Ocean City, MD, USA

Abstract

The Advanced Light Source Upgrade (ALS-U) to a diffraction-limited storage ring with a small vacuum chamber diameter requires excellent orbit stability and a fast response orbit interlock for machine protection. The on-axis swap-out injection scheme and dual RF frequencies demand fast monitoring of pulsed injection magnets and a novel approach to timing. Recent development efforts at ALS and advances in PLLs, FPGAs, and RFSoCs that provide higher performance and mixed signal integration can be leveraged for instrumentation solutions to these accelerator challenges. An overview of preliminary ALS-U instrumentation system designs and status will be presented.

INTRODUCTION

The ALS-U upgrade project will deliver a world-leading light source that provides users with bright, high-coherent-flux soft x-rays. The scope of the upgrade includes a new 2-GeV, high-brightness storage ring (SR) fed by a new full-energy accumulator ring (AR) and transfer lines in the existing ALS storage-ring tunnel. The AR will be installed early, and the plan is to complete AR commissioning in 2025, with the remaining accelerator sections to be commissioned in 2026.

The new diffraction-limited SR with a small vacuum chamber diameter requires excellent orbit stability and a fast response orbit interlock for machine protection. The on-axis swap-out injection scheme and dual RF frequencies demand fast monitoring of pulsed injection magnets and a novel approach to timing.

The ALS-U Instrumentation team is responsible for high speed, high performance electronic systems and fast data networks that interconnect devices. The systems are grouped into four categories: orbit stability (BPMS and fast orbit feedback (FOFB)), timing (event generation and distribution, injection triggering), fast machine protection (fast interlock and global mitigation), and fast data acquisition (fast monitoring of ICTs, BCMs, fast magnets).

Since the AR and SR requirements and interfaces for these systems are generally similar, the approach is to provide common designs with a superset of features to accommodate both rings. This paper will present a brief overview of each of the instrumentation systems.

* Work supported by the Director, Office of Science, Office of Basic Energy Sciences, of the U.S. Department of Energy under Contract No. DE-AC02-05CH11231
† jmweber@lbl.gov

ARCHITECTURE

To reduce the engineering effort required to implement these systems, a philosophy based on design reuse is employed wherever feasible. Examples of this include: identical hardware designs for the AR and SR, common PC boards and internal chassis components, and common panel components (i.e., connectors, displays, buttons, labels). In addition, modular firmware and embedded software are reused to minimize porting code across platforms and applications.

Many of the ALS-U instrumentation hardware designs use the Marble [1] digital platform, developed at LBNL. There are two versions of the Marble design sharing many common features: 'Marble', a higher-end version with a Kintex-7 FPGA, and 'Marble-Mini', a moderate performance version with an Artix-7 FPGA and reduced I/O channels. RFSoC platforms that integrate high speed data converters (DACs and ADCs) with programmable logic and dedicated CPUs in a single chip are used in the highest performance analog front end designs. Fast acquisition systems use the Xilinx ZCU111 RFSoC platform [2], while the Xilinx ZCU208 [3] is being evaluated for use in BPM electronics.

ALS-U Instrumentation systems use a network-attached device (NAD) model, in which electronic devices communicate with soft IOCs over a simple Ethernet UDP interface, as shown in Fig. 1. The architecture is flexible in that the number of soft IOCs required to support devices and how they are connected can be adjusted to trade off network bandwidth, CPU performance, and maintenance complexity.

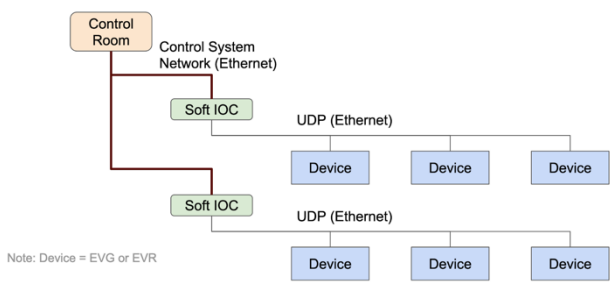

Figure 1: Example network-attached device (NAD) architecture.

ORBIT STABILITY

Orbit stability instrumentation includes FOFB and BPM systems, based on existing ALS designs [4]. The FOFB architecture is shown in Fig. 2. Each sector contains a cell controller that collects all the local sector BPM position data, sends the data on the FOFB network to all other cell

ISBN: 978-3-95450-214-1 ISSN: 2673-5490 doi:10.18429/JACoW-IPAC2021-WEPAB321

controllers, collects all position data from other cell controllers, calculates the local corrector power supply setpoints, and sends them to the local corrector power supply controllers (PSCs).

Figure 2: FOFB system architecture block diagram, including cell controllers, BPMs, and corrector PSCs.

The cell controller is based on the existing ALS design with some minor modifications. The chassis includes a Marble board and a pilot tone generator board. The Marble performs the fast orbit feedback response matrix calculation, computes PSC setpoints, and provides all the high-speed serial transceiver interfaces for the FOFB, BPM, and corrector PS fast data networks. It also provides control of the pilot tone generator PLL/clock distribution components via I2C serial bus. The pilot tone generator provides pilot tone frequencies above and below the master oscillator RF frequency on 12 individually controlled outputs.

The BPM architecture is shown in Fig. 3. BPM electronics are calibrated during accelerator operation using pilot tones. Each pilot tone generator provides pilot tone signals for each BPM in the sector. The pilot tone combiner assembly splits the pilot tone 4 ways and combines a split pilot tone with each button signal. The combined button + pilot tone signals are then sent to the BPM electronics for acquisition and processing.

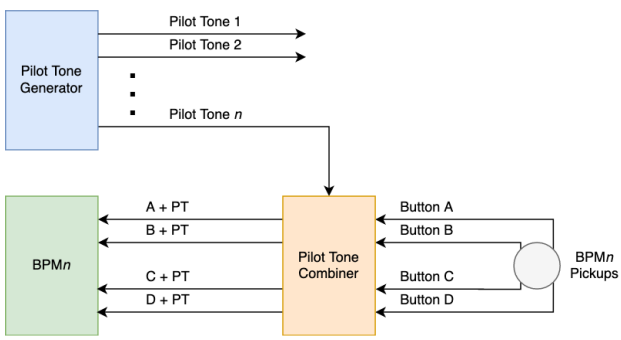

Figure 3: BPM system block diagram, including BPM readback electronics, pilot tone generator, and pilot tone combiner.

For the BPM electronics, an architecture based on the Xilinx Zynq UltraScale+ RFSoC ZCU208 evaluation platform is being evaluated. The ZCU208 contains eight 14-bit 5GSPS ADCs, so it is capable of providing readback for up to 2 button sets. The analog front end (AFE) section is based on the ALS design, with some minor modifications under consideration, including a new PLL with wider frequency range, and new band pass filters with wider bandwidth, higher frequency, and simplified mounting on the PC board.

TIMING

The timing system architecture is shown in Fig. 4. All event hardware, including Event Generator (EVG), Event Fanout (EVF), and Event Receiver (EVR) chassis are designed by LBNL. Since the existing ALS injector sections (Gun, Linac, Booster ring) remain after the ALS-U upgrade, the timing event protocol must be compatible with existing ALS timing system hardware [5] in the injector.

The new ALS-U accelerator sections will operate at a different RF frequency than the injector, where. the relationship is $f_{RF1} = \frac{608}{609} \times f_{RF2}$. Separate event generation logic and event stream distribution is required for each RF frequency. RF coincidence detection allows injection synchronization between the sections. To minimize the number of optical-electrical conversions, the first level of event stream fanout for each RF frequency is performed inside the EVG chassis, and each fanout level provides up to 35 outputs.

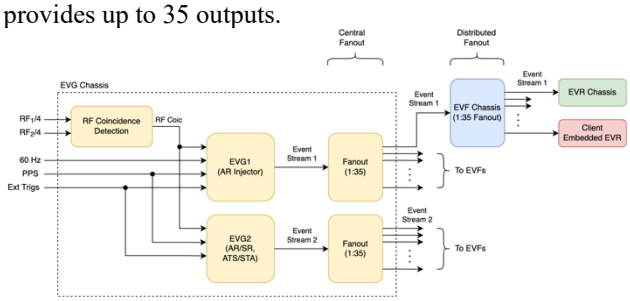

Figure 4: Timing system architecture block diagram, including separate event stream generation and distribution for two RF frequency domains.

The EVG and EVF designs include a common I/O board designed by LBNL with an Analog Devices 40x40 crosspoint switch [6] and Samtec FireFly [7] high density optical module interfaces, plus FS optical MPO-LC cassettes [8] to provide the 1:35 fanout capability. The EVR design uses a clock distribution PLL chip and 50 Ohm drive circuits to provide low jitter coax clocks and triggers to timing clients without embedded EVRs.

The new EVG prototype was temporarily installed and tested at ALS, and demonstrated to provide equivalent operation to the production EVG system, including injecting beam with nominal efficiency into desired target buckets in the storage ring.

ISBN: 978-3-95450-214-1 ISSN: 2673-5490 doi:10.18429/JACoW-IPAC2021-WEPAB321

FAST MPS

The Fast MPS architecture is shown in Fig. 5. Fast MPS sector nodes and mitigation node are designed by LBNL. The Fast MPS system must provide 100 µs time response mitigation for orbit interlock, beamline front end fast valves, and vacuum cold cathode gauge interlocks. The system also provides global mitigation for slow (PLC-based) interlocks. Sector nodes aggregate local sector signals and transmit them to the mitigation node via the fast MPS serial data network on fiber. The mitigation node collects all sector node interlock data, performs the interlock logic, and provides mitigation by removing the RF drive permit.

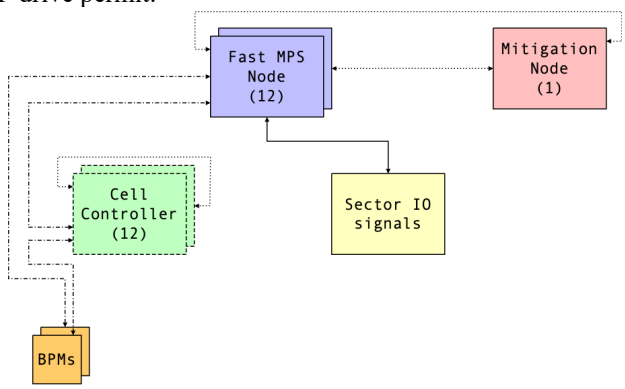

Figure 5: Fast MPS system architecture block diagram, including sector nodes and mitigation node.

FAST ACQUISITION

The fast acquisition system provides monitoring for ICTs, BCMs, and fast magnets. ALS-U will use hardware designs developed for and installed at ALS. The primary hardware will be the High Speed Digitizer (HSD) [9], which uses a Xilinx ZCU111 and an LBNL-designed analog front end, as shown in Fig. 6. One alternative is to use the Xilinx XM500 balun front end provided with the ZCU111 evaluation kit, currently in use as a BCM at ALS.

CONCLUSION

The instrumentation system designs are at a preliminary stage, and prototypes are planned to be completed by the end of the year. The final designs are planned to be completed early 2022 followed by the beginning of production procurement and build. A solid design philosophy based on hardware and code reuse provides confidence that these designs will meet the project requirements.

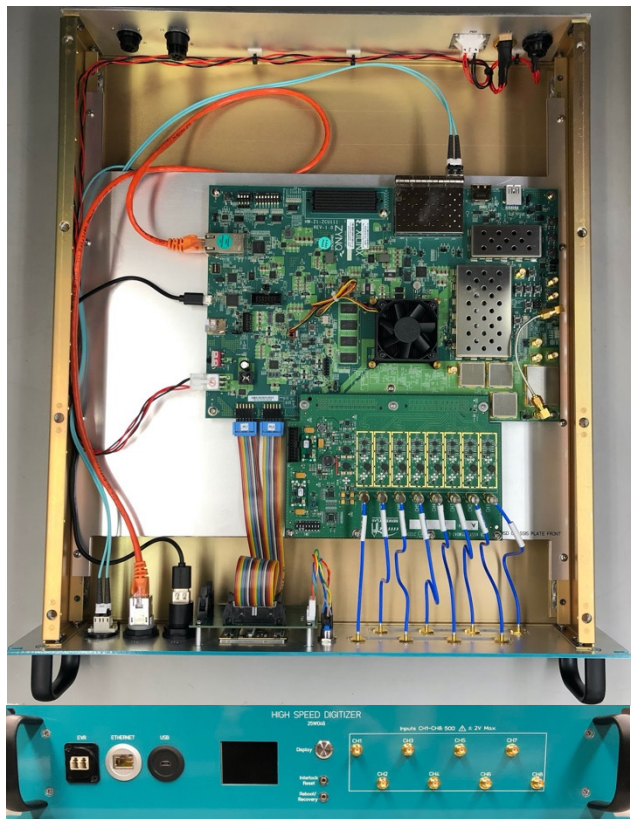

Figure 6: HSD chassis top view (top) and front view (bottom).

REFERENCES

[1] Berkeley Lab/Marble, https://github.com/BerkeleyLab/Marble

[2] Zynq UltraScale+ RFSoC ZCU111 Evaluation Kit, https://www.xilinx.com/products/boards-and-kits/zcu111.html

[3] Zynq UltraScale+ RFSoC ZCU208 Evaluation Kit, https://www.xilinx.com/products/boards-and-kits/zcu208.html

[4] G. J. Portmann, M. J. Chin, W. E. Norum, and J. M. Weber, "BPM Electronics with self-calibration at the ALS", presented at IBIC'20, Santos, Brazil, Sep. 2020, paper FRAO03, unpublished.

[5] J. M. Weber *et al.*, "ALS Timing System Upgrade," in *Proc. IBIC'14,* Monterey, CA, USA, Sep. 2014, paper MOPD18, pp. 187-190.

[6] Analog Devices, ADN4605, https://www.analog.com/en/products/adn4605

[7] FireFly™ Active Optical Micro Flyover System™ Cable Assembly, https://www.samtec.com/products/ecuo

[8] FHD Customized Pre-terminated Plug-play MPO Optic Cassette, https://www.fs.com/products/82482.html

[9] J. M. Weber, *et al.*, "Advanced Light Source High Speed Digitizer", in Proc. *IBIC'20*, Santos, Brazil, Sep. 2020, pp. 132-135. doi:10.18429/JACoW-IBIC2020-WEPP16