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STATUS OF DIGITAL BPM SIGNAL PROCESSOR FOR SHINE*

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Abstract

Digital signal processors that can handle 1 MHz bunch rate BPM signal processing is under development for SHINE. Two different processors have been developed at the same time, including an intermediate frequency signal processor with a sampling rate higher than 500 MHz, which can be used in general BPM applications; and a direct RF sampling processor, which can directly sample the C band cavity BPM signal without analog down-conversion modules and greatly simplifies the cavity BPM system. This paper will introduce the design, development status and performance evaluations of the processors.

INTRODUCTION

Shanghai HIgh repetitioN rate XFEL and Extreme light facility (SHINE) is a 3 km long hard X-ray FEL facility under construction in Shanghai. The designed beam repetition rate is 1 MHz. There are three types of BPMs locate at different sections of the machine, including stripline BPMs at injector and the gaps between superconducting accelerator sections, cold button BPMs in superconducting accelerator modules, and cavity BPMs in distributors and FEL sections. The required BPM system resolution is 10 μm, 50 μm and 200 nm at 100 pC respectively.

SHINE's BPM electronics include separate RF front-end modules and digital signal processors. Different RF front-end modules will be designed to meet the signal characteristics requirements of different BPM types, but all BPMs will use the same digital signal processors. The processor mainly contains ADCs for sampling, FPGA for signal processing and ARM for system control and communication. Considering the beam dynamic range, the relative resolution of the processor should be better than 0.1%.

The processor is designed as a 1 U height standalone instrument. With advances in electronic technology, today's FPGAs not only contain richer logic resources and faster data links, but also integrate hard ARM cores on the chip. This makes the FPGA a fully functional digital signal processing platform and makes it easier to design standalone instruments. At the same time, ADCs with sampling rate higher than 500 MHz and resolution higher than 12 bits are becoming more widely used. The high-speed serial interface JESD204B with data rates of up to 12.5 Gbps makes high-density data transmission between ADC and FPGA possible. The ADCs and FPGA are located on two PCB boards and are connected via FMC connector.

Except for the basic data acquisition (DAQ) function, the processor contains another FMC connector for a WRN timing board, SFPs for fast data transmission, DDR for large amount data capture and interlock output. The processor will run Linux OS and integrate EPICS IOC for data communication.

In recent years, direct RF sampling ADCs whose bandwidth greater than 6 GHz, sampling rate higher than 1.5 GHz, and resolution greater than 12 bits have begun to appear. It is mainly used for receivers in radar systems and communications and is ideal for direct sampling of C band cavity BPM signals. The RF-sampling processor can digitize RF signals directly without converting analog frequency to a lower intermediate frequency. Systems with direct RF sampling ADCs no longer require LO synthesizers, mixers, IF amplifiers, and IF filters for a typical superheterodyne receiver, reducing RF noise components, costs, design complexity, receive size, weight, and power, while improving the software programmability and flexibility of the system [1]. A direct RF sampling processor is also being developed to explorer the application of direct RF sampling technology in cavity BPM signal processing.

Therefore, two types of processors are designed for SHINE, intermediate-frequency (IF) processor and direct-RF sampling (RF) processor. Table 1 lists the specifications of the processors to be developed.

Table 1: DBPM Specifications

Parameter	Value
Channels	4
Bandwidth	≥1GHz/ ≥6GHz
ADC bits	≥12
Max ADC rate	≥ 500MSPS/≥ 1500MSPS
FPGA	Xilinx Zynq Ultra+MPSoC
Clock	Ext./Int.
Trigger	Ext./Self/Period
SFP	≥2
Interlock	Lemo
DDR	≥512MB
Software	Arm-Linux/EPICS
Relative resolution	≤0.100%

IF PROCESSOR

The development of the IF processor including two parts, one is the commercial boards that evaluate the performance of the ADCs, and the other is the development a fully new processor.

Xilinx evaluation board ZCU102 is selected as the carrier board for performance evaluation. ZCU102 contains a Zynq Ultrascale+ MPSoC FPGA XCZU9EG, two FMC connectors [2]. FMC boards with domestic ADCs and

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abroad ADCs are both evaluated. Domestic ADC (Fig. 1 left) is 12 bits, and abroad ADC (Fig. 1 right) is 16 bits. Figure 1 shows the system picture (up), ENOB (middle) and the spectrum of sampled data when input 50 MHz sine signal (bottom). The performance of the two is equal.

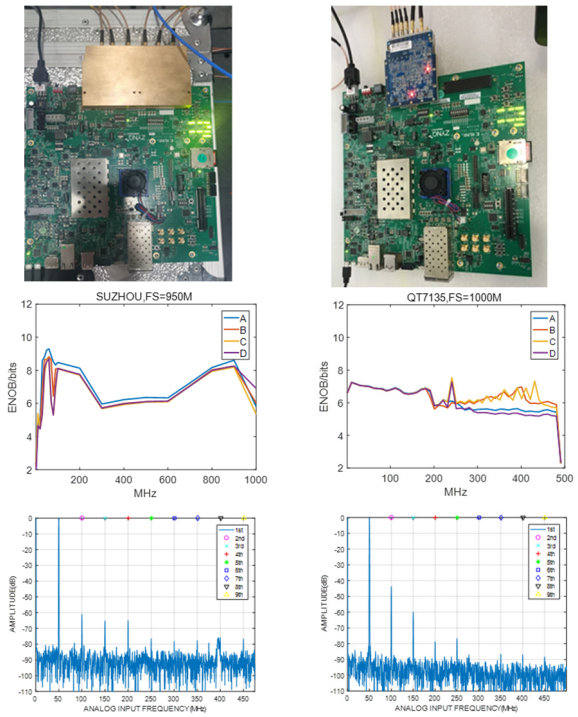

Figure 1: Lab evaluation of domestic(left) and abroad(right) ADCs.

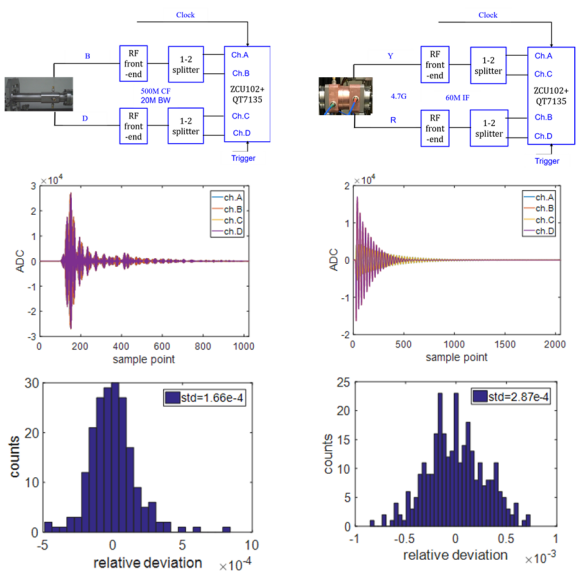

Figure 2: Relative resolution evaluations of stripline BPM(left) and cavity BPM(right) electronics on SXFEL beam.

The relative resolution tests of the evaluation board are carried on SXFEL stripline BPM (Fig. 2 left) and cavity BPM (Fig. 2 right). Figure 2 shows the test block diagram (up), sampled waveform(middle), and the results of RMS resolution. The ADC sampling rate is 952 MHz, that is 8 times of 119 external clock, which is synchronized to the SXFEL RF clock. The relative resolution of the electronics system for stripline BPM and cavity BPM is 0.016% and 0.029% respectively. That is much better than the requirement.

At the same time, a fully new designed processor is developed. Figure 3 (up) is the block diagram of the processor. It using the same FPGA as ZCU102 but ADC is 14 bits. Figure 3 (bottom) is the inside picture of the processor.

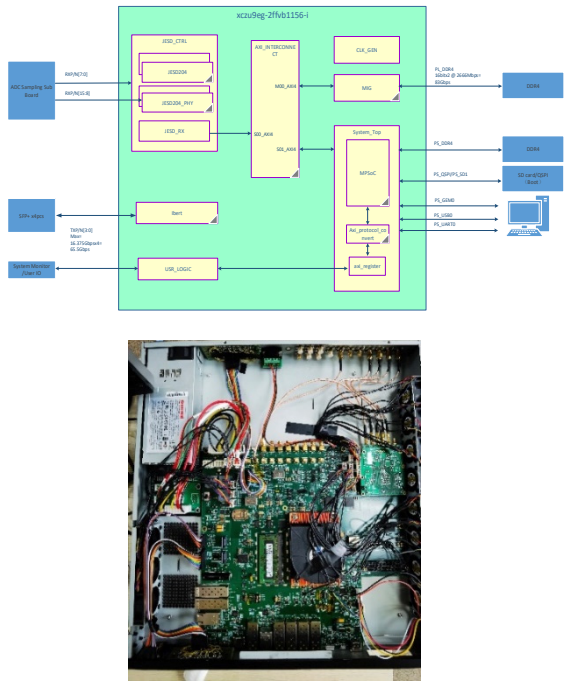

Figure 3: Block diagram(up) and picture(bottom) of the new developed processor.

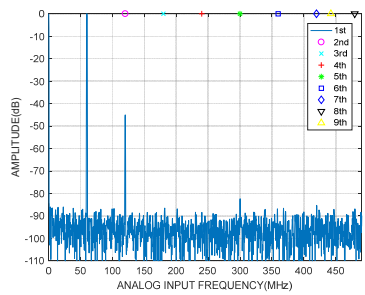

Figure 4: Block diagram(up) and picture(bottom) of the new developed processor.

Figure 4 is the spectrum of sampled data when input 60 MHz sine signal. The performance looks slightly better than the commercial boards.

RF PROCESSOR

A commercial 2 channels direct RF sampling ADC FMC board is used for cavity BPM signal processing evaluation.

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The bandwidth is 8 GHz and maximum sampling rate is 3.2 GSPS.

Figure 5 is the picture of the ADC board (left) and the measured ENOB (right). Figure 6 is the block diagram of SXFEL beam test. Figure 7 (left) is the sampled cavity BPM signal waveform. Figure 7 (right) is the relative resolution error VS. data processing size, the result is better than 0.040%.

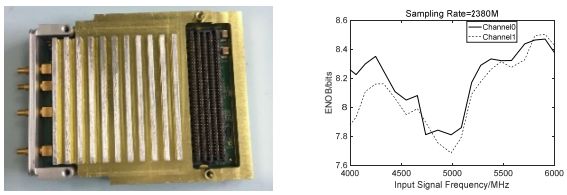

Figure 5: Direct RF sampling ADC card(left) and the ENOB result(right).

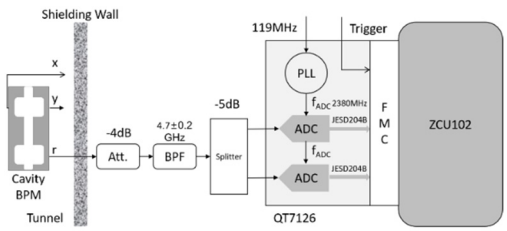

Figure 6: Test block diagram of RF processor.

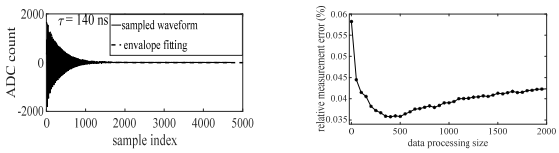

Figure 7: Sampled cavity BPM signal waveform(left) and relative resolution VS. data processing size(right).

Currently, a four channels RF processor is under development and almost done, progress will be introduced in future.

DIGITAL SIGNAL PROCESSING IN FPGA

The processor is designed to supplies 5 types of data, including capture raw ADC data, capture full rate results, streaming full rate results for feedback, decimated streaming results and decimated streaming raw ADC data. Figure 8 is the block diagram of the digital signal processing in FPGA.

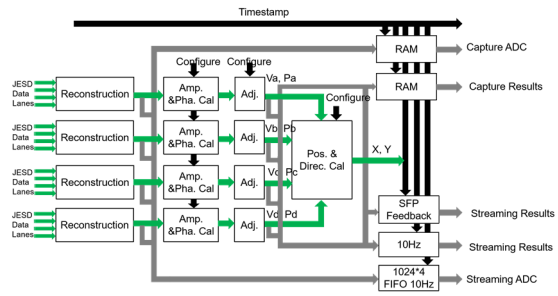

Figure 8: Block diagram of digital signal processing.

Spectrum analyzing (FFT) is always used in the cavity BPM signal processing [3]. However, FFT calculation is time-consuming and resource-intensive in FPGAs, it does not meet the 1 MHz repetition rate calculation requirements in SHINE. Hilbert transform can also be used to obtain envelops and phases of cavity BPM signals. It is easy to use in Matlab off-line data analyzing, but it is complexing and not suitable for FPGA implementation. Fortunately, Hilbert filter can be used to approximating Hilbert transform with reasonable number of taps [4]. Figure 9 shows the power spectral density of the original cavity BPM ADC data, the result after Hilbert transform, and the results with Hilbert filters approximating when different numbers of filter order and transition width are used. Figure 10 is the calculated amplitude envelop of cavity BPM signal from Hilbert transformation and Hilbert filter approximating. Both match each other very well.

The Hilbert filter coefficients are zero-valued and negative symmetry, after exploiting the characteristics and using pipeline structure, the filter can be realized with high efficiency. Then results can be got at each clock period after system latency in FPGA, 1 MHz rate calculation is entirely possible.

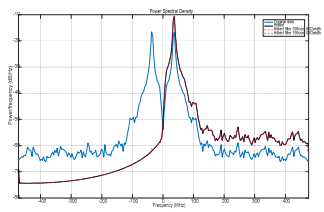

Figure 9: Comparison of power spectral density.

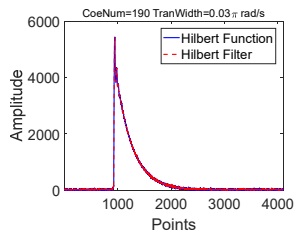

Figure 10: Envelope of cavity BPM signal.

SUMMARY

Two types of processor prototypes are developed for SHINE, including IF processor and RF processor. Domestic and abroad 1 GSPS ADCs are evaluated in lab and SXFEL, relative resolution of both is much better than 0.100%. New designed IF processor is ready. The relative resolution of direct RF sampling ADC is better than 0.040%, and can be used for CBPM RF signal sampling. A new RF processor is almost done. Digital beam signal processing algorithm is studied. Hilbert filter can be used for 1 MHz beam repetition rate calculation.

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