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INDUCTIVE ADDER PROTOTYPE FOR FCC-hh INJECTION KICKER SYSTEM

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Abstract

The future circular collider (FCC) requires a highly reliable injection kicker system. Present day kicker systems often rely on thyratron-based pulse generators and a pulse forming network or line: the thyratron is susceptible to self-triggering. Hence, an alternative pulse generator topology, based on fast semiconductor switches, is considered for the FCC. One possibility is an inductive adder (IA). A prototype IA has been designed and built: the main challenges are the fast rise time, high output current, low system impedance and a 2.3 µs pulse duration combined with low droop. This paper presents the results of measurements on the prototype IA where the rated output current and output voltage were achieved separately. Suggested improvements to the IA hardware are identified and proposals are presented that could help improve the kicker system performance.

INTRODUCTION

Solid-state pulse generators are an interesting alternative to thyratron based pulse generators such as pulse forming lines (PFL) and pulse forming networks (PFN). This applies especially for future accelerators such as the FCC, where the beam injection energy is too high to accept the risk of erratic triggering.

The inductive adder (IA) is a semiconductor based pulse generator. It consists of stacked layers of 1:1 transformers: the primary winding of each layer contains pulse capacitors and semiconductor switches. The secondary winding passes through all transformer cores and is connected to the load. If all primary circuits are triggered at the same time a fast rise time high voltage pulse is induced at the output of the secondary winding. An advantage of the IA compared with other topologies such as the Marx generator is that all semiconductor switches can be referenced to ground. Furthermore, the IA is a modular device that can be adapted to various voltages or currents by scaling the number of layers in the stack or the number of parallel branches per layer, respectively.

Modulation of the output waveform of the IA makes it possible to reduce ripple and droop of the output pulse. As shown in [1, 2] a pulse flattop stability of $\pm 0.02\%$ has been achieved in the laboratory. Tests and measurements in an accelerator showed similar results [3, 4].

In addition to the application of an IA for future particle accelerators, existing pulse generators can also be replaced by IAs [5]. Maintenance of old pulse generators becomes increasingly difficult since thyratrons and high voltage (HV) cables are expensive and sometimes difficult to source. Additionally, some PFLs use SF6-gas insulated cables which, for environmental reasons, should be replaced [6]. Hence, the IA is a very promising solution to replace these cables and design a pulse generator with increased reliability and performance and also for the challenges of future colliders.

PROTOTYPE DESIGN

The baseline design for the FCC-hh is an injection energy of 3.3 TeV, with the LHC as a high energy booster (HEB) [7]. The injection kicker system requirements for the FCC-hh are presented in [8], and are summarized in Table 1.

Table 1: Injection Kicker Requirements With LHC as HEB

Parameter	Unit	Value
Field flat-top pulse length	µs	2.0
Field rise time definition	%	0.5-99.5
Field rise time	ns	430
Field fall time	µs	<1
Field flat-top ripple	%	$\pm$0.5
Repetition rate	Hz	10

Based on the requirements shown in Table 1, a prototype IA was designed. From the available 430 ns of field rise time, 355 ns are foreseen as magnet fill time and the remaining 75 ns as the rise time of the output pulse of the IA [9]. Oil was selected to insulate the 15 kV output voltage and realise the low characteristic impedance of 6.25 Ω, while keeping the diameter of the magnetic cores within an acceptable range [10]. PSpice simulations showed that for the required field flattop duration of 2.0 µs and the field rise time of 430 ns, a current pulse flattop duration of 2.3 µs is sufficient. The relatively long pulse duration of 2.3 µs was achieved by biasing the transformer cores into the third quadrant of the BH curve, and therefore doubling the available flux swing. Biasing is also important to keep the height of the IA stack small, to achieve short rise time. The envisaged parameters for the design of the full-scale IA are shown in Table 2.

The detailed prototype design steps and measurements carried out on sample components are presented in [11]. The assembly and first measurements on a small scale prototype are presented in [12]. In [13] two PCBs were used per primary winding, with up to 12 parallel branches per PCB. In the latest design, there are 12 PCBs per primary winding with two parallel branches per PCB [10]: alternatively, each layer can be equipped with only one or more PCBs, depending upon the required current pulse. In this way a high flexibility to assemble the prototype test setup with a

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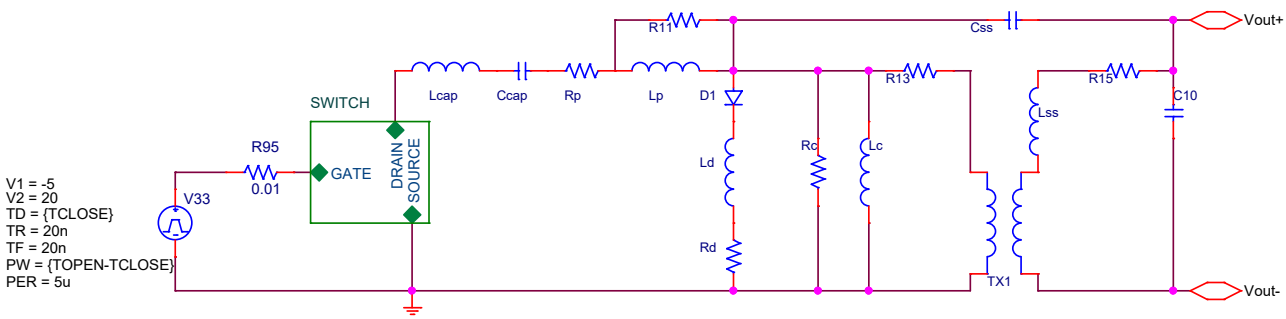

Figure 1: Schematic of an IA layer, as represented for PSpice simulations.

Table 2: Envisaged Parameters for a Full-Scale Prototype IA

Parameter	Unit	Value
System impedance	Ω	6.25
Output current	kA	2.4
Output voltage	kV	15
IA output pulse length	µs	2.3
Number of constant voltage layers	-	19
Number of parallel branches per layer	-	24
Number of modulation layers	-	3
Voltage per layer	V	960
Current per branch	A	~100

limited number of PCBs is achieved, to generate pulses with various voltage and current values.

CIRCUIT MODEL

An important part of the IA prototype design process was the simulation and optimization of the circuit with PSpice. The equivalent circuit of a layer of the IA is based on the circuit and simplifications presented in [14]. The model of one layer consists of a pulse capacitor, MOSFETs, free wheeling diodes, equivalent circuit of the magnetic core and components to represent parasitic effects of the geometry.

Figure 1 shows the schematic of an IA layer, as represented for PSpice simulations. The subcircuit named SWITCH in Fig. 1 consists of an appropriate number of MOSFETs modelled in parallel. The gate resistor of each MOSFET model is included in the subcircuit. Depending on the simulation, the number of parallel MOSFETs in the subcircuits needs to be adapted: furthermore the capacitance of the pulse capacitor Ccap and the primary inductance Lp is changed accordingly. For comparison with the measurements presented in the next section, two parallel MOSFETs, a total capacitance of 50 µF and an inductance of 11 nH were simulated per PCB: the value of 11 nH was measured with a network analyzer for a PCB with two parallel branches [10]. Css and Lss of Fig. 1 represent the parasitic capacitance and inductance of the coaxial structure of the IA [14]. In reality Css and Lss are distributed over the length of each layer however, they are modelled as lumped elements per layer. The value of Css and Lss are calculated from the dimensions of the coaxial structure and insulation material characteristics:

$$C_{ss} = \frac{2\pi \cdot \varepsilon_0 \varepsilon_r \cdot l}{\ln \frac{d_o}{d_i}}, \; L_{ss} = \frac{\mu_0 \mu_r \cdot l \cdot \ln \frac{d_o}{d_i}}{2\pi}, \qquad (1)$$

where l is the axial length of a layer, d_i the inner and d_o the outer diameter of the insulation, ε_0 and ε_r the specific and relative permittivity, respectively, and μ_0 and μ_r the specific and relative permeability, respectively, of the insulation. For the prototype, Css is 135 pF and Lss is 350 pH per layer. Measurements from the secondary winding, with a network analyzer, showed that the total inductance, with each PCB replaced by four equally spaced short-circuits, is ~80 nH for 22 layers [10]. Hence, an inductance of 36 nH was modelled at each end of the stack, in series with the secondary winding, to account for the inductance of HV connectors etc., to obtain a total of 80 nH (22·350 pH+2·36 nH = 79.7 nH). Since the output waveform was measured on a 22 layer prototype with 15 constant voltage layers and 7 layers in short-circuit, the simulation model consisted of 15 constant voltage layers and 7 layers with a resistor of 0.1 mΩ in parallel to Lc, representing a short-circuit. Further measurements and simulations were conducted with one layer and 24 parallel branches to obtain an output waveform of ~2.4 kA and ~1 kV. Predicted output waveforms are compared with the measurements in the next section.

MEASURED OUTPUT WAVEFORM

Magnetic cores with a square shaped BH curve were used in the layers, as described in [11], and a dc current of 0.7 A was applied to bias the cores to the third quadrant of the BH-curve. The pulse length was set to 2.32 µs for the measured and predicted waveforms.

As shown in Table 2, the IA was designed with 19 constant voltage layers and 24 parallel branches per layer. However, with the available number of PCBs, 15 layers could be equipped with 2 parallel branches. Hence, with a voltage of 1 kV per layer, an output voltage of ~15 kV could be achieved. A load resistor of 50 Ω results in a current of ~150 A in each MOSFET. To compare the predictions with the measurements the model was adapted to the measurement setup in terms of the number of parallel MOSFETs and layers, as described in the previous section. The capaci-

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tor charging voltage was 1025 V: with this value the pulse output flattop voltage did not drop below 15 kV (Fig. 2).

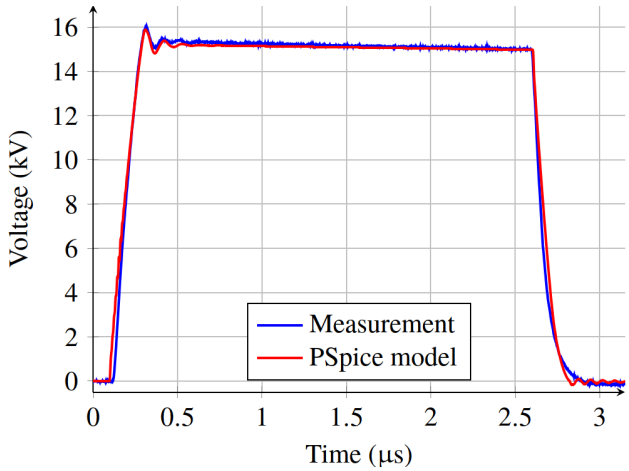

Figure 2: Comparison of predicted and measured output pulse of nominally 15 kV into a 50 Ω load.

Figure 2 shows the measured and predicted output pulses and Table 3 compares the parameters of these pulses. Generally the MOSFET model provided by the supplier, as used in the complete PSpice model of the IA, results in reasonable agreement with measurements. However, the rise time of the predicted waveform is slightly longer and its overshoot is lower. The differences between the waveforms could be caused by inaccuracies of the impedance measured with the network analyzer: the primary inductance of the circuit has a relatively big influence on the rise time and the overshoot of the waveform [10].

Table 3: Measured and Predicted Pulse Parameters for 15 kV Into a 50 Ω Load

Parameter	Unit	Measured	PSpice Model
t_{rise} 0.5-99.5%	ns	162	186
t_{rise} 1-99%	ns	156	183
t_{rise} 10-90%	ns	122	149
Average flattop	kV	15.2	15.1
Overshoot	V	742	587
Ripple	%	±3.9	±3.0
Ripple frequency	MHz	11.1	8.9
t_{fall} 90-10%	ns	140	140

Further measurements were carried out on one layer with 24 parallel branches to generate pulses with the nominal current of 2.4 kA: the load resistance was 0.4 Ω. Due to the increased L/R time constant with the low load resistance, to obtain high output current, the rise time is significantly longer and no overshoot occurs. Figure 3 shows a comparison of the predicted and the measured output waveforms of one IA layer charged to 1 kV pulsing into a 0.4 Ω load. Table 4 compares the measurement and prediction. The measured waveform shows a lower flattop than the predicted waveform: this could be due to, e.g., the MOSFETs having a higher on-state resistance than in the model or the load resistor might have a negative voltage coefficient. The measured rise and fall times are shorter than the those predicted, as already noted in the case of the 15 kV measurements.

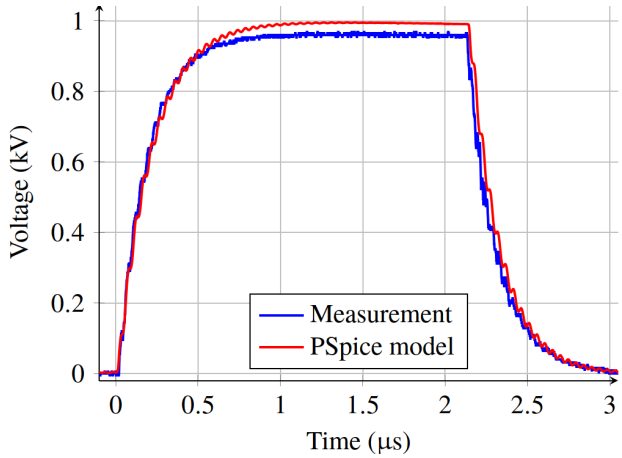

Figure 3: Comparison of measured and predicted output pulse of nominally 1 kV into a 0.4 Ω load.

Table 4: Measured and Predicted Pulse Parameters for 1 kV Into a 0.4 Ω Load

Parameter	Unit	Measured	PSpice Model
t_{rise} 0.5-99.5%	ns	838	944
t_{rise} 1-99%	ns	699	852
t_{rise} 10-90%	ns	357	452
Average flattop	V	952	993
t_{fall} 90-10%	ns	370	408

Since the measured and predicted waveforms shows reasonable agreement, for both the 15 kV and the 2.4 kA sets of measurements, the PSpice model is considered to be verified and hence can be used for the design of the full-scale IA.

CONCLUSION

An IA prototype for the FCC injection kicker system was designed and constructed. The secondary winding was insulated with oil to reduce the dimensions of the magnetic cores. To further reduce the required volume of magnetic material, and achieve an output pulse with fast rise time, a biasing circuit was used. To achieve fast switching and high current, SiC MOSFETs were used. Measurements and predictions of the output pulse of the IA show reasonable agreement. Hence, since the pulse requirements for the FCC injection kicker system were obtained with the PSpice model of the full scale IA, it looks feasible to reach the specified parameters. Nevertheless, further investigations are required to achieve the specified flattop ripple and compensate flattop droop, by using modulation layers, as well as to achieve the pulse rise time for high current pulses in the full-scale design. An increased system impedance of 8.33 Ω is recommended to achieve faster rise times and increase the insulation gap to the secondary winding.

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