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DEVELOPMENT OF A 166.6 MHz LOW-LEVEL RF SYSTEM BY DIRECT SAMPLING FOR HIGH ENERGY PHOTON SOURCE

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Abstract

A digital low-level radio frequency (LLRF) system by direct sampling has been proposed for 166.6 MHz superconducting cavities at High Energy Photon Source (HEPS). The RF field inside the cavities has to be controlled better than ±0.1% (peak to peak) in amplitude and ±0.1° (peak to peak) in phase. Considering that the RF frequency is 166.6 MHz, which is well within the analog bandwidth of modern high-speed ADCs and DACs, direct RF sampling and direct digital modulation can be achieved. A digital LLRF system utilizing direct sampling has therefore been developed with embedded experimental physics and industrial control system (EPICS) in the field programmable gate array (FPGA). The performance in the lab has been characterized in a self-closed loop with a residual peak-to-peak noise of ±0.05% in amplitude and ±0.03° in phase, which is well below the HEPS specifications. Further tests on a warm 166.6 MHz cavity in the lab are also presented.

INTRODUCTION

High Energy Photon Source (HEPS) is a 6 GeV diffraction-limited synchrotron light source with a kilometer-scale circumference currently under construction in Huairou, Beijing [1]. Its main beam parameters are listed in Table 1.

Table 1: Main Parameters of HEPS

Parameter	Value	Unit
Beam energy	6	GeV
Beam current	200	mA
Circumference	1360.4	m
Beam power	900	kW

A double-frequency radio frequency (RF) system has been proposed with 166.6 MHz as the fundamental accompanied by an active third harmonic system [2]. The current layout of the RF system is shown in Fig. 1. Both systems utilize superconducting RF cavities [3], driven by solid-state power amplifiers and controlled by digital low-level RF (LLRF) systems. The required RF field stability inside cavities is ±0.1% (peak to peak) for the amplitude and ±0.1° (peak to peal) for the phase. RF parameters of HEPS are listed in Table. 2.

There are two ways to process the signal from the cavity in the digital LLRF system, as shown in Fig. 2(a) and (b)

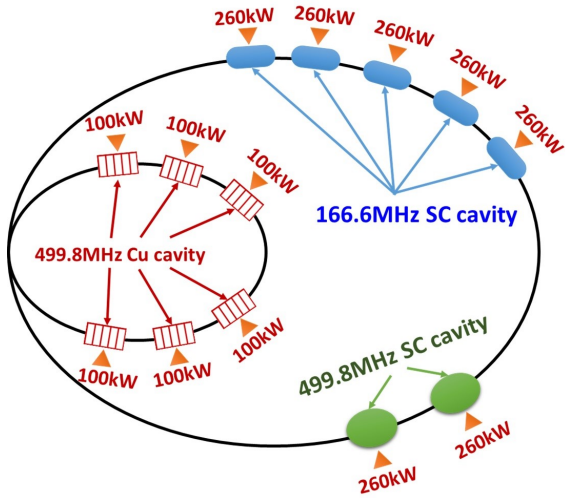

Figure 1: Layout of HEPS RF system.

Table 2: Main Parameters of HEPS RF System

Parameter	Main RF	Harm. RF	Unit
Frequency	166.6	499.8	MHz
# of Cavities	5	2	-
Operating Temp.	4.2	4.2	K
Cavity voltage (V_c)	1.2	1.75	MV
R/Q	139	95	Ω
RF power/cavity	180	200	kW
# of RF source	5	2	-
RF power/source	260	260	kW
RF source type	SSA	SSA	-
Amplitude stability	±0.1%	±0.1%	-
Phase stability	±0.1°	±0.1°	-

respectively. The traditional method shown in Fig. 2(a) is heterodyne field detection, which requires a down conversion process. The boards developed in HEPS-Test Facility (HEPS-TF) utilize this method [4]. The second method shown in Fig. 2(b) is direct sampling, which does not require any down conversion process. Compared with the traditional LLRF system based on the down-conversion scheme, the system of direct sampling eliminates the down converter, and makes the system much simpler and smaller, and the absence of a down-converter can also minimize the temperature dependency. But It will be sensitive to the clock jitter.

Considering that the RF frequency is 166.6 MHz, which is well within the analog bandwidth of modern high-speed

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ADCs and DACs, direct RF sampling and direct digital modulation can be achieved. A digital LLRF system utilizing direct sampling has therefore been developed.

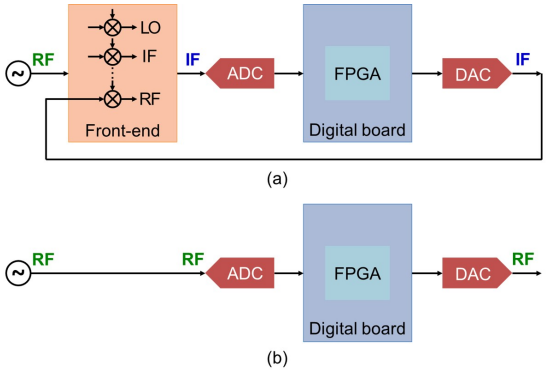

Figure 2: Simplified diagram of a digital LLRF system: (a) Down conversion and (b) direct sampling.

In this paper, the configuration of the digital LLRF system utilizing direct sampling is shown. And the result of performance test in lab is also presented.

LLRF SYSTEM ARCHITECTURE

Hardware

The hardware of the digital LLRF system based-on direct sampling mainly consists of a high-speed AD/DA board, a digital signal processing board, a frequency synthesizer, and a low-speed AD/DA board, as shown in Fig. 3.

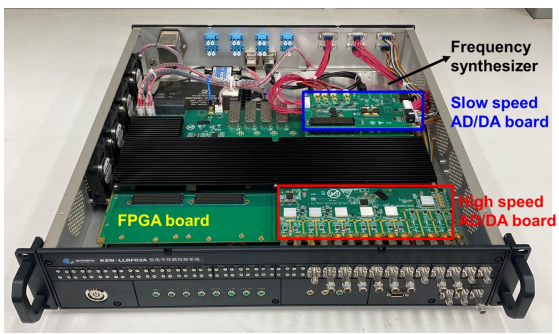

Figure 3: The 166.6 MHz digital LLRF system based-on direct sampling.

The high-speed AD/DA board consists of five 16-bit, 2-ch ADCs (ADS42LB69) of more than 250 MSPS, and one 16-bit,4-ch DAC (DAC38J84) of more than 1.3 GSPS. In order to obtain the amplitude and phase directly from the sampling, the clock frequency should be synchronized with the RF frequency. The direct-sampling LLRF system uses the frequency synthesizer and a clock divider (LMK04828) to achieve this function. The frequency synthesizer is mainly composed of a voltage controlled oscillator (VCO), a phase detector (PD) and a filter. In addition, The FPGA board is mainly composed of XILINX XC7VX690TFFG1761-2 and XILINX XC7Z100FFG1156-2. The FPGA board is used to realize the functions of digital IQ demodulation, digital signal processing algorithms and fast data logging for post mortem analysis. XC7Z100FFG1156-2 can be applied to develop the embedded experimental physics and industrial control system (EPICS). The low-speed AD/DA board is used control the tuning system (tuner and piezo).

Control Loops

Field quality inside a cavity is an essential parameter for an accelerator RF system which directly affects the performance of the beam. LLRF system is used to maintain the amplitude and phase of the accelerating field inside cavities by a set of feedback control loops. These loops are usually implemented in the FPGA. In the LLRF system based-on direct sampling, RF signals were firstly sent to ADCs for data acquisition. With the IQ demodulation algorithm, the respective in-phase and quadrature (I/Q) vector signals were achieved. After the I/Q vector rotation of pickup signal from the cavity, a narrow band cascaded integrator and comb (CIC) filter is used as a low pass filter. The error between the set point and the pickup value was respectively sent to the Proportional and Integral (PI) controller. The I and Q signals of the PI controller were sent to the DAC, and the DAC directly generates the RF signal. The output RF signal was then used to excite the solid-state amplifier.

TEST IN THE LAB

Clock Jitter

The LLRF system with direct sampling is more sensitive to the clock jitter compared to a traditional LLRF system with down conversion. An under-sampling scheme is used for the RF detection in the LLRF system based-on direct sampling. We measured the phase noise of the ADC sampling clock. In our case, the ADC input (f_{in}) was 166.6 MHz and the sampling frequency (f_s) was 95.2 MHz (f_s=8*f_{RF}/14). It is difficult to directly measure the clock jitter of the ADC sampling clock, so we measured the signal from the frequency synthesizer (8*f_{RF}) and its RMS jitter was 78 fs with a frequency offset range of between 10 Hz and 10 MHz which is shown in Fig. 4.

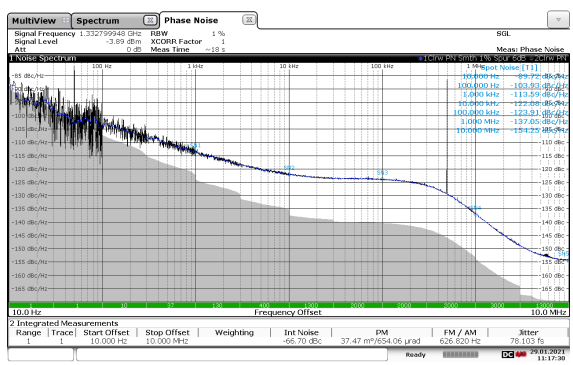

Figure 4: Sampling clock phase noise measurement.

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Tests on a Warm Cavity

The digital LLRF system utilizing direct sampling was connected to a warm 166.6 MHz cavity in the lab to fully characterize the entire system. The setup is shown in Fig. 5. Two antennas were mounted on the cavity ports to be used as coupler and pickup. The cavity system has a loaded bandwidth of 80 kHz. The cavity was driven by the RF signal directly output from the DAC, and the cavity field signal was extracted by the pickup and connected to the ADC(ADC1). The stability of this cavity system was then measured. The system was up and running for 60 minutes with a field set value ref_amp=0.8. The residual noise is shown in Fig. 6. The field inside the cavity can be regulated with a stability of 0.0075% (rms) in amplitude and 0.0055° (rms) in phase, largely excelling the required value. A summary of the main results is listed in Table 3.

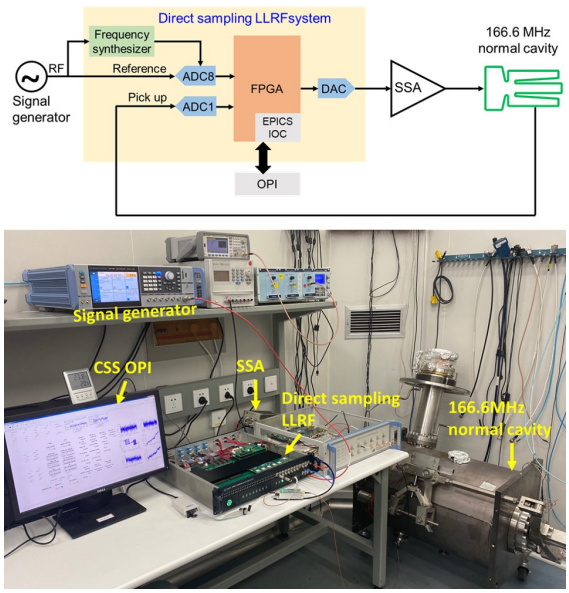

Figure 5: The LLRF test stand with a warm 166.6 MHz cavity.

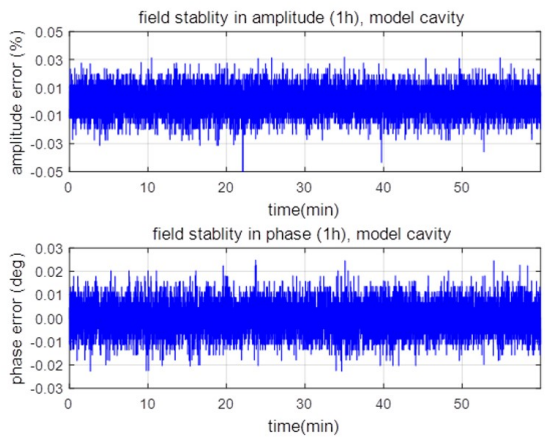

Figure 6: Amplitude and phase error measured on a warm cavity with ref_amp=0.8. Errors are referring to differences between feedback and reference signals.

Table 3: Field Stability (rms) Measured in Short-Term (0.68 ms) and Long-Term (60 Minutes) on a Warm Cavity

	Amplitude stability	Phase stability
Short term	0.0065%	0.0055°
Long term	0.0075%	0.0055°

SUMMARY

This paper describes the architecture of the 166.6 MHz LLRF system based-on direct sampling scheme. Excellent control stabilities were demonstrated on the cavity in the laboratory. The performance in the lab has been characterized by a residual peak-to-peak noise of ±0.05% in amplitude and ±0.03° in phase. The results well satisfy the HEPS specifications.

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