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A KLYSTRON PHASE LOCK LOOP FOR RF SYSTEM AT TPS BOOSTER RING

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Abstract

In TPS booster ring, the DLLRF is used to controlled the ramping gap voltage and also the energy saving module is applied to save power in top-up mode. But a problem of PI controller saturation due to a large phase change occurred to us when the energy saving module worked. The energy saving module switches the anode voltage of the klystron from high to low level to decrease the cathode current while the ring does not inject and do the opposite while the ring injects. This action causes a large phase change of the transmitter and leads the PI controller to work in the wrong direction. We add a klystron phase loop to solve this situation.

INTRODUCTION

The TPS was designed to operate at 3 GeV, a frequency of 500 MHz, a gap voltage of 2.8 ~ 3.5 MV and a beam current of 500 mA. When TPS is in top-up mode, the beams inject from the booster ring to the storage ring about 2 ~ 5 mA for every 4 minutes to keep the beam current at setting level. The time for injection is about 3 ~ 7 seconds while the booster ring is operated at 900 kV gap voltage with ramping mode. In the other time, the gap voltage of the booster ring remains at 100 kV. Therefore, the klystron does not need to always work at full power. Energy saving module is used to regulate the cathode current by changing the anode voltage setting. As the recording data of our utility group, this module can save maximum power about 797 MWh every year.

However, the properties, including the gain and phase shift, of klystron change when the cathode current is different. These changes all depend on the compensation of PI controller to keep the gap voltage and phase as the setting. Our digital low level RF (DLLRF) control system is based on IQ sampling [1-3], thus the phase calibration is important to avoid PI controller work in wrong polarity. If the phase shift of RF system loop changes after calibration, it causes a phase shift between PI controller output and input. Under this phase asymmetry, the output I or Q gets into saturation easily when PI controller works near to full power. Therefore, it is a critical situation of PI controller at the moment of klystron cathode current changing. We add a klystron phase lock loop (KPLL) to solve this problem.

PHASE VARIATION

TPS storage ring is operated at top-up mode to maintain the beam currents at setting level. Before the moment of beam injection, the energy saving module [4-5] increases the anode voltage of klystron to pull up the cathode currents for high RF power output. It leads the phase of transmitter changing for ~ 7 seconds. As shown in Fig. 1, ADC phase represents the phase of cavity operated around 60° when beams inject. DAC phase shows that DLLRF must regulate the phase of output signal to keep the electric field of cavity with a correct phase. Total time of this injection is 6 seconds from 3 to 9 sec. The cathode current of klystron increases from 1.87 A to 5.0 A at ~ 2.6 sec and comes back to 1.87 A at ~ 9.6 sec. As the changing of cathode current, the transmitter phase has a large jump from 82° to -2° at ~ 2.6 sec and the other jump from 61° to 142° at -9.6 sec. PI controller covers all phase shift. Under such phase asymmetry between the input and output of PI controller, the stability of gap voltage gets worse. For example, the ADC phase has spikes about 3 degrees at every ramping cycles. Some injection fails happen during the situation of unstable phase and it takes more ramping cycles to get enough injection beams.

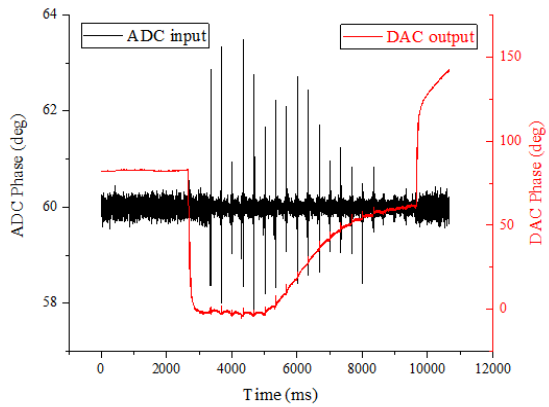

Figure 1: Phase variation of ADC and DAC of DLLRF without KPLL while beam injections.

KPLL ARCHITECTURE

KPLL function is designed to fix the phase shift of klystron due to the cathode current variation and it is based on FPGA in DLLRF system. The architecture of DLLRF is showed in Fig. 2. The calibration function is used to cancel the phase shift cause by the whole loop static delay. The calibration degree is the compensation angle of the difference between θ_{Pt} and θ_{out} at non-feedback mode (PI controller output is constant). The KPLL is put in front of IQ modulator and used to compensate the dynamic phase shift due to the klystron (or the transmitter) which works in different conditions, including low/high power and various cathode currents. KPLL only works when RF system is operated in feedback mode.

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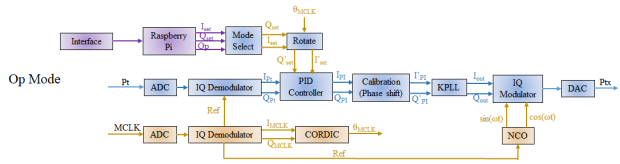


Figure 2: DLLRF architecture of the TPS.

KPLL needs to monitor the output of the transmitter to discover the phase shift. As shown in Fig. 3(a), the signal P_f and P_t are the power signals coupled from the transmitter output and cavity, respectively. In Fig. 3(b), PI controller regulates the output by the error between Pt and setting value. The output phase, θ_{PI}, is calculated by coordinate rotation digital computer (CORDIC) and compared with θ_{Pf}. If the difference θ between θ_{PI} and θ_{Pf} is different from the initial θ_0, it means that a phase shift occurs to RF system. The position of phase shift is at the path between DLLRF output and transmitter output. According to the variation of θ, KPLL can provide the dynamic compensation angle for the transmitter under the different cathode currents while RF system is in feedback mode.

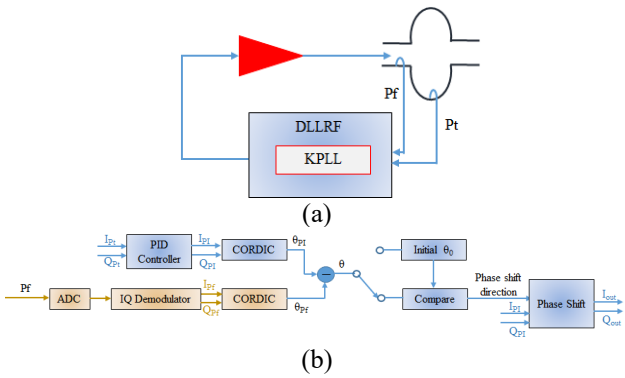
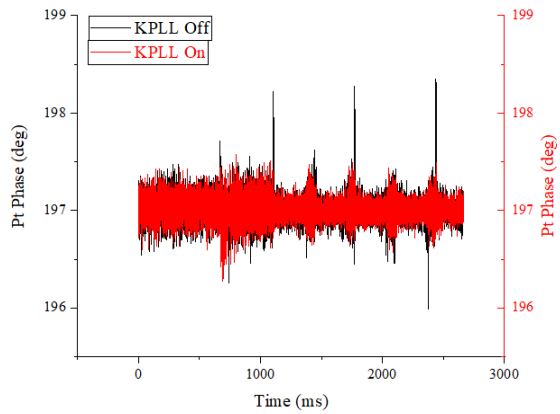


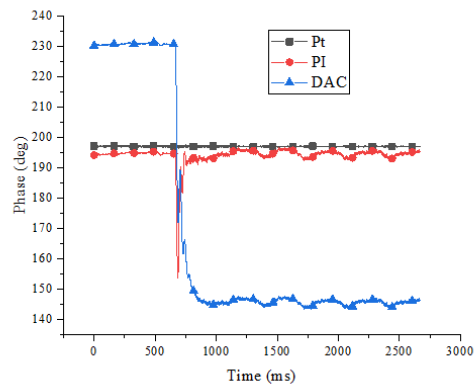
Figure 3: (a) The simple schematic loop of DLLRF system. (b) The logic blocks of KPLL.

EFFECT OF KPLL

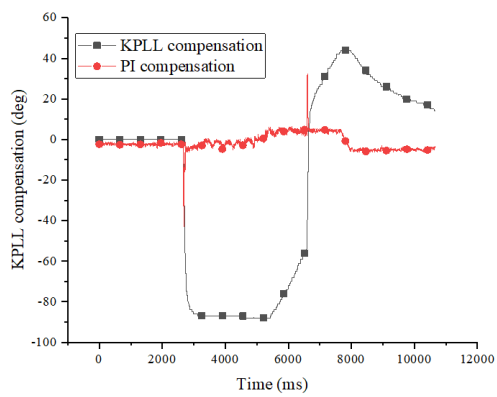
There are some data of TPS BR cavity phase while KPLL turn on/off shown in Fig. 4. In Fig. 4(a), the transmitter increases the cathode current at 700 ms, the gap voltage begins to ramp at 1100 ms, and also θ_{Pt} has spikes at every ramping cycles. The spikes of θ_{Pt} with KPLL on are smaller than those with KPLL off. The maximum phase spike is about 3° with KPLL off and it reduces to 0.35° with KPLL on. Figure 4(b) shows the phase of Pt, PI, and DAC output with KPLL on. θ_{Pt} represents the phase of cavity and it keeps stable at 198°. θ_{PI} is the output signal phase of PI controller and it has a large drop about 40° at 700 ms and comes back immediately. θ_{DAC} is the final output signal phase of DLLRF system and it has a large change from 230° to 145° at 700 ms. The drop of θ_{PI} means the PI controller provides temporary compensation for the klystron phase change until the KPLL gives enough phase compensation. The phase change of θ_{DAC} represents the total phase compensation about 85°. Figure 4(c) shows the phase compensations of KPLL and PI controller in an injection period. The injection stars from 2800 ms and stops at 6900 ms. The transmitter cathode current raises from 1.87 A to 5.0 A while injection period and then comes back. The curve of KPLL phase compensation fits to the phase change of klystron. Because the speed of KPLL is 1°/ms, the PI controller gives temporary compensation about -40° at the star of injection and about 30° at the end.



(a)



(b)



(c)

Figure 4: The phase data of TPS BR cavity. (a) The θ_{Pt} with KPLL on/off. (b) θ_{Pt}, θ_{PI}, and θ_{DAC} with KPLL on while energy saving switching. (c) The phase compensation of KPLL and PI controller.

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POWER CONSUMPTION

The energy saving module of TPS BR decreases the power consumption of transmitter by regulating cathode current (Icc). Before the KPLL function is applied to DLLRF, Icc can be set as 4.71 A while the ring is not injecting. As shown in Fig. 5, the standby power consumption of transmitter is 135 kW. If Icc is set as 2.86 A at standby period, the PI controller sometimes is easy to saturation or hang and affects the injection efficiency when Icc raises from 2.86 A to 5.0 A. After KPLL function is applied, the loading of phase compensation of PI controller decreases. PI controller can work smoothly while Icc raising and falling. We can set Icc as 1.87 A at standby and the power consumption is 62 kW.

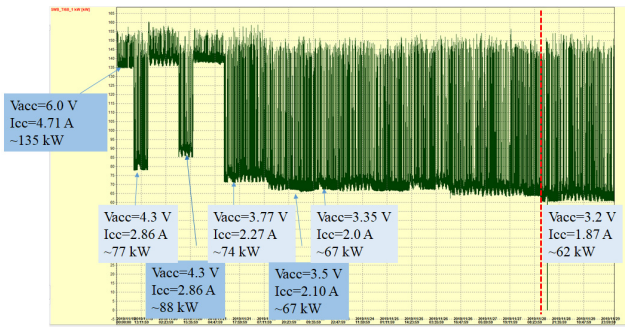

Figure 5: Power consumption of TPS BR RF system.

CONCLUSION

As the energy shortage in the whole world, the accelerator should work for decreasing power consumption. To regulate the cathode current of transmitter is a kind of method to avoid power wasting. Thus, a large phase change due to cathode current regulating is a challenge to the DLLRF system. In this study, the KPLL is developed for this issue and successful to stabilize the PI controller. In TPS BR RF system, there is ~ -88° phase change while the cathode current raises from 1.87 A to 5.0 A. KPLL provides the phase compensation and reduces the burden of PI controller. PI controller only supplies a temporary phase compensation about -40° and works smoothly while cathode regulating. Under this operating condition, the standby (not injecting) power consumption reduces from 135 kw to 62 kw. The maximum saving power is about 797 MWh a year.

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