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DEVELOPMENT OF A NEW INTERLOCK AND DATA ACQUISITION FOR THE RF SYSTEM AT HIGH ENERGY PHOTON SOURCE

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Abstract

A new interlock and data acquisition (DAQ) system is being developed for the RF system at High Energy Photon Source (HEPS) to protect essential devices as well as to locate the fault. Various signals are collected and preprocessed by the DAQ system and individual interlock signals from the solid-state power amplifier, low-level RF, arc detector, etc. are sent to the interlock system for logical decision to control the RF switch. The programmable logic controller (PLC) is used to collect slow signals like temperature, water flow rate, etc., while fast acquisition for RF signals is realized by dedicated boards with down-conversion front-end and digital signal processing board. In order to improve the response time, field programmable gate array (FPGA) has been used for interlock logic implementation with an embedded experimental physics and industrial control system (EPICS). Data storage is managed by using EPICS archiver appliance and an operator interface (OPI) is developed by using control system studio (CSS) running on a standalone computer. This paper presents the design and the first test of the new interlock and DAQ for HEPS RF system.

INTRODUCTION

High Energy Photon Source (HEPS), which consists of a linac, a booster and a storage ring, is under construction by the Institute of High Energy Physics. HEPS RF system comprises six 499.8-MHz normal conducting cavities in the booster, while five 166.6-MHz superconducting cavities and two 499.8-MHz third harmonic superconducting cavities in the storage ring [1]. The diagram of the RF system is shown as Fig. 1, which mainly consists of the solid-state power amplifier (SSPA), the power distribution system, the coupler, the cavity, the low-level RF (LLRF) system, the data acquisition (DAQ) and interlock system.

This paper focuses on the development of the DAQ and interlock system. The DAQ system is used to collect slow signals and RF signals, then output interlock signals after comparing with their thresholds. The interlock system accepts various interlock signals from different devices, then output control signals after the logical decision. The control system is developed based on the experimental physics and industrial control system (EPICS). All collected signals, interlock signals, as well as threshold settings are displayed by an operator interface (OPI) that is developed by the control system studio (CSS), while the data storage is accomplished by the EPICS archiver appliance.

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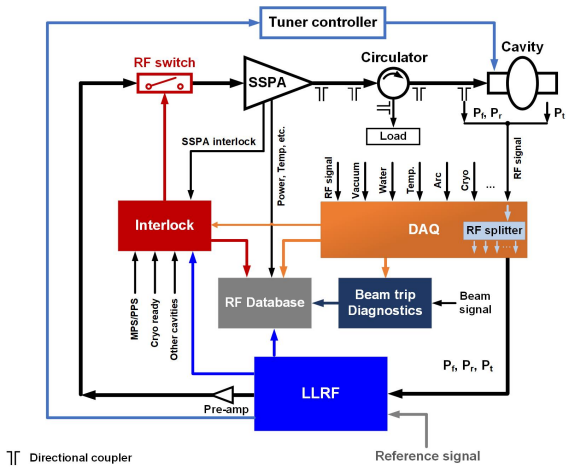

Figure 1: Diagram of the RF system.

DATA ACQUISITION SYSTEM

The DAQ system includes two parts, one is the slow signal acquisition which is accomplished by the programmable logic controller (PLC), and the other is the RF signal acquisition, which is realized by dedicated boards with down-conversion front-end and digital signal processing board.

Slow Signal Acquisition System

Slow signals comprise the vacuum pressure of the coupler and cavity, the forward and reflected power in different location of the transmission line, the temperature in different position of various instruments, the temperature, flow rate and pressure of the cooling. These signals are first collected, then acquired values of the temperature, pressure, and flow rate are subsequently compared with their thresholds, and interlock signals are produced whenever the value falls outside the permitted range.

Various PLC modules produced by the Yokogawa Electric are used to realize the collection of slow signals. The temperature signals are collected by the temperature monitoring module (F3CX04-0N). The data type of the flow rate and pressure is current, so they are collected by the analog input module (F3AD08-6R). The vacuum and power are first measured by the vacuum gauge and power meter respectively, and then collected by the ladder communication module (F3RZ82-0F). The output of interlock signals is completed by the TTL output module (F3YD32-1T). The control of the whole collection process is finished by the sequence CPU module (F3SP76-7S), while the real-time CPU module (F3RP71-1R) is used to run the EPICS [2].

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According to the number of signals, at least three PLC units are needed. Considering the extension of the system in the future, the slow signal acquisition system includes a main unit and three subunits, and the data transmission between the main unit and subunit accomplished by the FA-bus type 2 module ((F3LR02-1W). The PLC cabinet of the DAQ system is shown as Fig. 2. The slow signal acquisition system was tested, and each data could be collected correctly.

Figure 2: PLC cabinet of the DAQ system.

RF Signal Acquisition System

RF signals comprise the forward and reflected RF signal of the SSPA, load and cavity. For the booster, the frequency of RF signals is 499.8 MHz. Six RF signals first convert to intermediate frequency (IF) signals that is 15.61875 MHz through an analog front-end board, then sampled by analog-to-digital converters (ADCs), which the sample clock is 62.475 MHz. So, the in-phase and quadrature (I/Q) sequence of the signal are obtained. After the demodulation, average and cordic algorithm, the amplitude and phase of the RF signal can be acquired. At last, by comparing with the amplitude threshold, the interlock signal will be produced. The data of the amplitude, phase and threshold will be transferred between the computer and system on a programmable chip (SOPC) by the ethernet. The EPICS input-output-controller (IOC) is installed in the computer, and some calculation are completed by the IOC. The flowchart of the signal process is shown in Fig. 3.

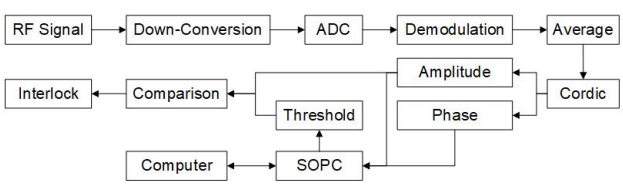

Figure 3: Flowchart of the signal process.

Dedicated boards with down-conversion front-end board and digital signal processing (DSP) board are used to collect RF signals. The front-end board has six down-conversion channels. The input reference signal is divided into four channels by the splitter. One of them is fed into the DSP board to produce the IF signal, then the IF signal is fed back to the front-end board and mixed with the reference signal to produce the local oscillator (LO) signal. At last, RF signals mixed with the LO signal to produce IF signals that is fed to ADCs [3].

The DSP board consists of a field programmable gate array (FPGA) chip and a variety of peripherals. The core FPGA chip is the Stratix III series that produced by Altera company. Peripherals include three 16-bits dual-channel high-speed ADCs, the clock generator AD9520-3, that provide the clock signal for the FPGA and ADCs, and other common devices like ethernet, flash, and so on. The complex programmable logic device (CPLD) is used to configurate the clock generator. The RF signal acquisition system is shown in Fig. 4.

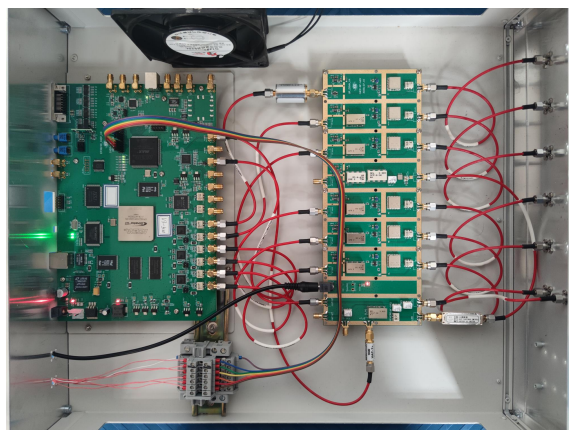

Figure 4: RF signal acquisition system.

To test whether the system can work properly, using the signal generator (SG) to output a 499.8-MHz RF signal, then the RF signal divided by the splitter into six RF signals, and feed the RF signal into each down-conversion channel. Changing the power of the RF signal, the measured and calculated power of each channel is shown in the Fig. 5. From Fig. 5, we can see the measurement result is corresponding with the signal generator output power well.

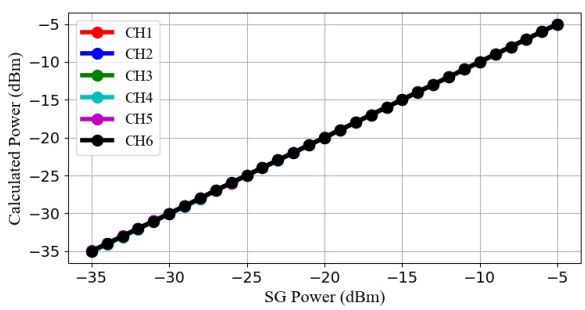

Figure 5: Measurement result.

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INTERLOCK SYSTEM

The interlock system is used to collect interlock signals from various of devices, such as the DAQ system, LLRF, SSPA, etc., then output tens of control signals after the logical decision. Because the type of interlock signals includes the TTL and LVTTL, the photoelectric isolating circuit is used to convert TTL signals to LVTTL signals, as well as the realization of the photoelectric isolation to prevent the interlock from triggering by mistake. Each channel can be blocked via dual in-line package (DIP) switches if required and a push-button is used to reset the system state when an interlock event happens. Block signals and the reset signal are switching signals, so a transformation circuit is needed to convert switching signals to LVTTL signals.

Output signals include the LED signals, cavity interlock signals, status signals, and control signals. The status of each channel is indicated by its own LED light with green for the normal state, red for the fault state, and flashing green if the channel is disabled. The booster has six cavities, as well as six interlock system. if one interlock system shut down the RF power, another five RF power also need to be shut down, this function is realized by the cavity interlock signals. Status signals which indicate the RF system operation status are send to the central room and the control signal is send to the RF switch.

Because plenty of input and output signals are needed, the commercial FPGA board can't meet the requirement, so the design and manufacture of the dedicated interlock board are inevitable. The diagram of the designed interlock board is shown as Fig. 6. The FPGA chip ZYNQ 7045 was chosen according the demand of the I/O pin number. Meanwhile, this FPGA chip is embedded with the dual ARM Cortex-A9 processor, so the chip plus a variety of peripherals, such as flash, ethernet, and so on, the development of the embedded linux system and EPICS is possible [4].

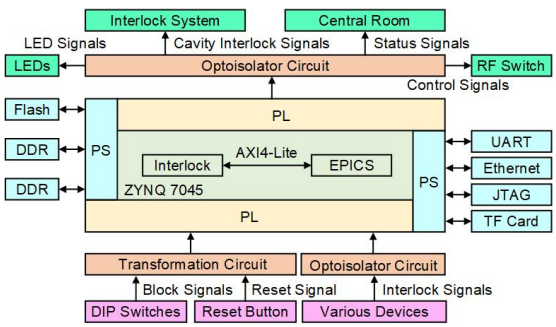

Figure 6: Diagram of the designed interlock board.

The designed and fabricated interlock board is shown as Fig. 7. Some tests were carried out and some problem were solved. At first, the program software Vivado couldn't connect to FPGA chip because the integrated circuit (IC) chip FT232H, which could be configured in a variety of industry standard serial or parallel interfaces like RS232, JTAG, and so on, wasn't configured in JTAG mode. Then the test program was downloaded, and each signal could input or output normally except the reset signal. After the carefully check, we found two related diodes were soldered backward. Up to now, the development of the interlock program was finished, and the development of the embedded linux system and EPICS will start in the next step.

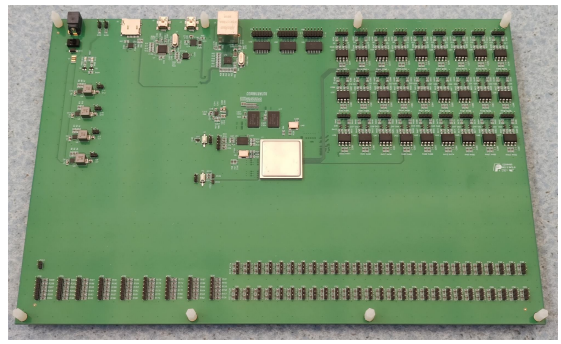

Figure 7: Picture of the interlock board.

FINAL REMARKS

A new data acquisition and interlock for the RF system at High Energy Photon Source (HEPS) was developed. The DAQ system, which includes the slow signal and RF signal acquisition system was constructed to monitor the operation status of various devices. The interlock board was designed and fabricated according to requirements of the RF system, and the interlock program was developed to collect the interlock signals from a variety of instruments, then output the control signals after the logical decision. The first test of the DAQ and interlock system was accomplished, and each subsystem worked as expected.

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