A NEW MODULATOR CONTROLLER OF THE PLS LINAC

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Abstract

The 2-GeV electron linac at Pohang accelerator laboratory (PAL) has been operated continuously as a full energy injector for the Pohang Light Source (PLS) since Dec. 1994. There have been continuous efforts to improve the klystron-modulator (K&M) system more stable and reliable. To improve self-diagnostic, operation, monitoring, and remote communication, we recently developed a new modulator controller based on an industrial PC platform. The modulator controller mainly consisted of an interlock signal conditioning module, a fast pulse signal-conditioning module, and the main PC platform. Operating system of the PC is Windows NT 4.0, and application software is developed with C++. The interlock signal-conditioning module generally carries digital and slowly varying clean analog signals. The fast pulse signal-conditioning module is used for pre-conditioning fast pulse and DC signals that inherently have high noise levels, such signals as a beam voltage, a beam current, an EOLC current, a HVDC voltage, and a HVDC current. All operation data of the K&M system can be acquired and saved in real time. We are upgrading the main PLS control system with EPICS. The industrial PC platform will function as an Input/Output Controller (IOC) in the future EPICS PLS control system.

1 INTRODUCTION

The PLS 2-GeV linac employs 12units of high power pulsed klystrons(80-MW) as the main RF sources. The matching modulators of 200-MW (400kV, 500A) can provide a flat-top pulse width of 4.4 μsec with a maximum pulse repetition rate of 120-Hz at the full power level. To have good phase stability of electron beams, the pulse-to-pulse flat-top voltage variation of a modulator requires to be less than ± 0.5 %. Annual operation hour of the K&M system is over 5000 hours. Accumulation of operation data of the K&M system is very important for beam operation and self-diagnostic. This paper describes development, installation and operation of the PLS linac new modulator controller.

2 KLYSTRON AND MODULATOR OF THE PLS LINAC

Major specifications of the modulator are listed in Table 1. Maximum repetition rate of the modulator is 180 Hz. However, normal operating rate is 30 Hz. Injection rate of the linac electron beam to the PLS storage ring is 10 Hz. The modulator can be divided into four major sections: a charging section, a discharging section, a pulse transformer tank, and a klystron load. In the charging section, a SCR AC-AC voltage regulator controls primary 3-phase 480 V AC power. The voltage regulator receives feedback signals from the primary AC voltage and current detectors, and also from the high voltage DC (HVDC) detector. The closed loop control of the AC-AC voltage regulator ensures stable HVDC output. The maximum HVDC is 25 kV. The pulse-forming network (PFN) is resonantly charged from the HVDC filter capacitor through the charging inductor and diode. The De-Q'ing circuit is installed at the charging inductor secondary to regulate the PFN charging voltage. Pulse-to-pulse beam voltage regulation is less than ± 0.5%. Two parallel, fourteen section, type-E Guillemin networks [3] are used for the PFN. The PFN impedance is about 2.8 Ω. Each PFN capacitor has a fixed capacitance of 50 nF, and each PFN inductor can be varied manually up to 4.5 μH. By adjusting inductance of each PFN section, we can precisely tune the flattop of the modulator output voltage pulse. The end of line clipper (EOLC) removes excessive negative voltage developed after discharge on the PFN capacitors as well as the thyratron. The klystron is Toshiba E3712 that provides 80 MW, 2856 MHz microwave output.

Table 1. Modulator Specification.

Description	Parameter
Peak Power	200 MW max.
Average Power	289 kW max./48 kW normal
Repetition Rate (PRR)	180 Hz max./30 Hz normal
Peak Output Voltage	400 kV
ESW	7.5 μs
Flat-top Width (<±0.5%)	4.4 μs
Charging Time	5.76 ms

3 A NEW MODULATOR CONTROLLER OF THE PLS LINAC

3.1 Signal Types and Operation Sequence of the K&M System

Table 2 lists signal types of the PLS linac K&M system. The signals can be categorized as analog monitor and control signals, digital monitor and control signals, and trigger signals. Total number of signals is 72 for one K&M system.

Table 2. Signal Types of the K&M System

TYPE		SIGNAL
Analog Monitor (8)		HVDC Voltage, HVDC Current Beam Voltage, Beam Current EOLC Current, Klystron Vacuum Gallery Vacuum, Tunnel Vacuum
Analog Control (1)		HVDC Reference
Digital Monitor	Dynamic Interlock (9)	HVDC Voltage, HVDC Current Beam Voltage, Beam Current EOLC Current, Klystron Vacuum Gallery Vacuum, Tunnel Vacuum SCR AC Over Current
	Static Interlock (48)	Heater, Cooling, Door, Safety, etc.
Digital Control (3)		Mod. On/Off, HVDC On/Off, Reset
Trigger (2)	Input	Modulator Trigger
	Output	Thyratron Trigger

Among eight analog monitor signals, five signals, excluding the three vacuum signals, contain high noise.

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Therefore, they require special attention before bring into the controller. We pre-condition the five noise signals and convert to clean digital signals before providing to the controller. Therefore, there are same signal names in the dynamic interlock signal list. The analog vacuum signals are also converted to digital at the controller and functions as dynamic interlock signals. As the modulator controller receives 'on' command, it initially checks interlock status before turns on HVDC. If all operating conditions are cleared out, it sets HVDC reference to run the modulator. During running, it continuously monitors all static, dynamic, and trigger interlocks. When it detects interlock signals, a typical action is SCR gate hold to block AC power supply. If the system has serious malfunction, the controller completely turns off the modulator and waits operators reset.

3.2 Configuration of the Modulator Controller Hardware

The new modulator controller of the PLS Linac consists of three major parts: an interlock signal conditioning module, a fast pulse signal-conditioning module, and a main PC platform. Fig. 1 shows a schematic block diagram of the modulator controller. The interlock signal-conditioning module is indicated with a dotted square in Fig. 1. The fast pulse signal-conditioning module deals with fast pulse and high level noise signals and also high noise DC signals. The main PC platform is consisted of an industrial PC, analog to digital conversion boards, and digital signal input/output boards.

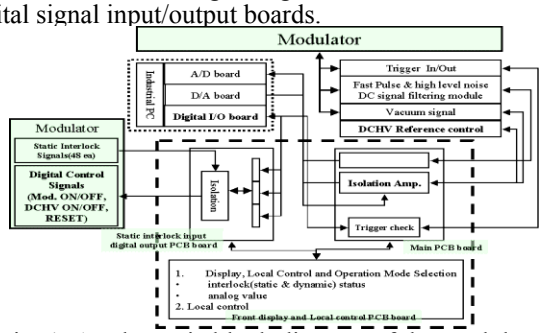

Fig. 1. A schematic block diagram of the modulator controller.

3.2.1 Interlock Signal Conditioning Module

The interlock signal-conditioning module generally deals with clean analog and digital signals. The module consists of three PCB boards. The first PCB receives static interlock signals, and also provides digital control signals to the modulator. In addition, it has connection with the digital in/out board to supply monitoring signals and receive commands from the PC platform. All static interlock and digital control signals are isolated with photo-couplers at the PCB to de-couple noise signals. The second part is a main PCB board. All analog and trigger signals are in and out from the main PCB board. Three vacuum analog signals are isolated with isolation amplifiers at the board. Other analog signals are pre-conditioned and isolated at the fast pulse signal-conditioning module, and then connected to the main PCB board. All analog signals are then converted to digital signals and provide them to the main PC platform as digital dynamic interlock signals. The third part is a front display and local control PCB board. This board functions to display analog and digital status of modulator, and to enable local control and operation mode selection.

3.2.2Fast Pulse Signal Conditioning Module

The fast pulse signal-conditioning module deals with very noisy and fast varying pulse and DC analog signals. Noisy and short pulse signals that are generated in the K&M system are beam voltage, beam current, EOLC current. Noisy and long pulse signal is HVDC current. Noisy DC signal is HVDC voltage. These five signals are categorized as dynamic interlock signals. Since the signals are very dynamic, the controller should be able to manage real time data. In addition, because of high noise level within the signals, they should be pre-conditioned before bring them to the clean environment controller area in order to avoid electrical malfunctions. Fig. 2 shows the fast pulse signal conditioning module block diagram. Input signal levels are adjusted at the signal divide. The inputted signals are sampled at multi-points to process. For long and short pulse signals, the sampling time is synchronized with an external trigger that also triggers the modulator thyratron. By receiving the synchronized trigger signal, the module generates sampling start and end time. The sampling start and end time can be adjusted to avoid high noise signal areas. For DC signals, the input signals are continuously sampled without synchronized trigger. The timing gaps between edges of the external trigger rise and edges of the sample start and the sample end can be varied from zero to 10 μs for short pulse acquisition, which they can be adjusted from zero to 10 ms for long pulse signal acquisition. The AD783, which is the employed sample and hold chip, has a typical acquisition processing time of 250 ns with 0.01 % accuracy. Four AD783 are employed for multi-point sampling.

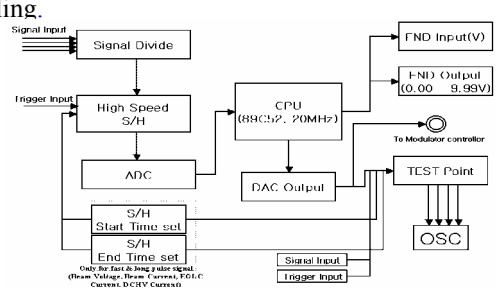

Fig. 2. The fast pulse signal conditioning module block diagram

The multi-sampled analog data are converted to digital with the ADC in Fig. 2. The CPU is then collect the digital data to calculate an average value. The value is then converted to an analog signal before providing it to the modulator controller. Noise signals are filtered during the process of multi-point sampling and averaging. All processed signals at the signal-conditioning module are isolated with isolation amplifiers before providing to the modulator controller. AD7893 is employed to convert analog to digital signal. The AD7893 has 12-bit resolution and 6 μs signal conversion time. AD7243 is employed to convert digital to analog signal. The AD7243 has 12-bit resolution and 4 μs signal conversion time at positive full-scale change. Therefore, total minimum data processing time of sampling is 11 μs. This time is short enough to process K&M signals. The isolation is not shown in Fig. 3. Fig. 4 shows a sample of such pre-conditioned waveform for high noise pulse signals. As can be seen in the figure, the high noise exists at the beginning of the

pulse. Therefore, we are able to avoid the noisy area by using the signal-conditioning module. Output signal in Fig. 3 has no noise in its content. Fig. 4 shows a sample of pre-conditioned waveform of HVDC voltage. As shown in the figure, all noise signals are removed during the process of sampling and averaging in the conditioning module.

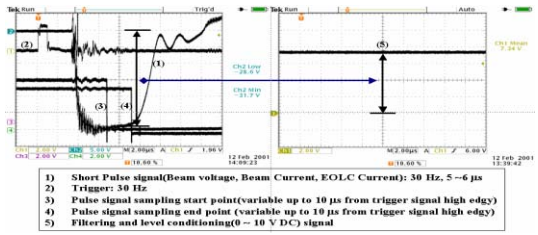

Fig. 3. Pre-conditioned waveform of short pulse signal (2 μs/div)

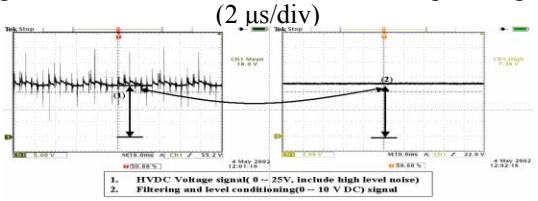

Fig. 4. Pre-conditioned waveform of HVDC voltage (10 ms/div)

3.2.3 Main PC Platform

For real time data acquisition and management of the K&M system, we use an industrial PC and in/out (I/O) boards. We select Windows NT as the operating system of the industrial PC to have system security and stability. We use Borand C++ builder 5.0 as the main language to write application programs. Table 3 lists major specifications of the main PC platform.

Table 3. Major specification of the main PC platform.

CPU	Intel Pentium III 866 MHz
Memory	PC-133 168 Pin 128 MB
HDD	IBM 36 GB SCSI, Ultra-wide 2
A/D Board D/A Board Digital I/O Board Serial Comm. B'd	PCL-816, 16 Ch, 16 Bit, PCL-816-DA, 2 Ch, 16 Bit PCL-722, 144 Digital I/O PCL-858, 8-Port High Speed RS-232
Operating System Language	Windows NT 4.0 + Service Pack 6.0 Borand C++ Builder 5.0

3.3. Configuration of the Modulator Controller Software

As mentioned, main programming language of the modulator controller is Borand C++ builder 5.0. Application program runs with timer event method in order to control and monitor the modulator. The application program is consisted of five routines: main routine, timer-AD-read routine, timer-static-read routine, timer-display routine, and timer-save routine. Message handling time in windows application programs is generally dependent on hardware configuration. Minimum event time of the modulator controller application program is tested with the modulator controller hardware configuration. Without sub-routines, minimum event time in windows application programs is typically 20 ms. With the modulator application program sub-routines, the minimum event time is measured as 30 ms. In order to gain program stability and reliability, We decide the minimum event time of the modulator controller as 50 ms. Since the modulator runs with 30 Hz repetition rate, the 50 ms minimum event time is satisfactory to detect any modulator operation status within two consecutive events. The modulator operation mode can be selected as local or remote. In local operation mode, the modulator is controlled at the interlock signal-conditioning module. The PC platform is the control center for the case of remote operation mode. The PC always manages real time data regardless of operation mode and generates and saves operation data files. Saved data files are analog value file, dynamic interlock file, static interlock file, and analog signal analysis file. We have a plan to upgrade the main PLS control system with EPICS [4]. Therefore, the PC platform of a new modulator controller can function as an input-output controller (IOC) in the future EPICS PLS control system. We will program standard mod-bus TCP format and RS232 communication format for the modulator control system. Fig. 5 shows connection diagram of the modulator control system with mod-bus TCP.

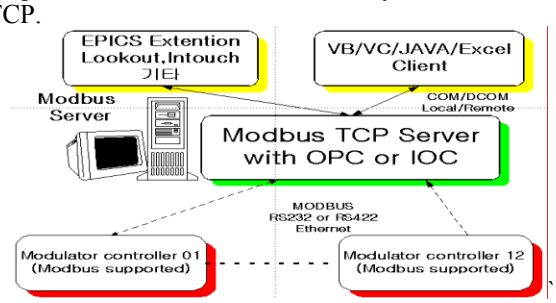

Fig. 5. Connection diagram control system with mod-bus TCP

4. SUMMARY

A new modulator controller is developed for the PLS Linac klystron and modulator system. The modulator controller can diagnose and manage operation data of the K&M system in real time. The controller is based on an industrial PC platform. The most difficult task in realizing such controllers is to condition high noise signals. We develop a new method to effectively process such high noise signals. We installed twelve controllers as of May 2002. The new modulator controller will be fully operational by Dec. 2002. The modulator controller will function as an IOC of EPICS when the currently pursuing EPICS main control system upgrade is completed.

5 REFERENCES

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