THE DESIGN AND PERFORMANCE OF THE SPALLATION NEUTRON SOURCE LOW-LEVEL RF CONTROL SYSTEM *,**

M. Champion, M. Crofford, K. Kasemir, H. Ma, C. Piller, Spallation Neutron Source, Oak Ridge National Laboratory, Oak Ridge, TN, USA
L. Doolittle, C. Lionberger, M. Monroy, A. Ratti, Lawrence Berkeley National Laboratory, Berkeley, CA, USA
J. Power, H. Shoee, Los Alamos National Laboratory, Los Alamos, NM, USA

Abstract

The Spallation Neutron Source (SNS) linear accelerator low-level RF control system has been developed within a collaboration of Lawrence Berkeley, Los Alamos, and Oak Ridge national laboratories. Three distinct generations of the system, previously described, have been used to support beam commissioning at Oak Ridge. The third generation system went into production in early 2004, with installation in the coupled-cavity and superconducting linacs to span the remainder of the year. The final design of this system will be presented along with results of performance measurements.

INTRODUCTION

The LLRF controller for the SNS linac has been designed with a collaborative effort among three US national laboratories, Oak Ridge, Lawrence Berkeley and Los Alamos.

The three main components of the SNS LLRF Control System are the RF field control module (FCM), the High Power Protection Module (HPM), and the reference system. The HPM and the reference systems have been described elsewhere.

The FCM is a digital feedback controller that uses a Field Programmable Gate Array (FPGA) for fast data processing. The work presented here covers the test performance and production of the field control module.

The FCM is the result of the evolution of the FPGA-based data acquisition and processing systems developed for the SNS project by Los Alamos and Berkeley[1].

The SNS project is currently under construction. The equipment described here has been used during beam commissioning of the front end and DTL systems, and is ready to support CCL commissioning. The beam commissioning for the entire linac is planned for 2005.

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PROTOTYPING AND TESTING

Throughout the project, we took a gradual and incremental approach towards accomplishing our goals. As a consequence of this decision, we leveraged from the experience of the first and second-generation LLRF systems, as well as that of similar components in the BPM system[2].

Shortly after deciding on the basic approach, we designed and built a prototype system, which we used for debugging and performance testing purposes[3,4]. This system was used to power up both a superconducting RF system, using the JLAB SRF cavity test stand, and a warm system at SNS.

The prototype system was an expansion over the interim system built at Berkeley and used as a benchmark and a development platform for the final system[5]. This allowed us to compare most of the performance measurements and make the necessary adjustments to enhance performance as described below before going into final production.

PRODUCTION EXPERIENCE

Once the system was successfully prototyped, we went to commercial production. In this process we combined the fabrication of the FCMs with that of the HPMs and requested that the vendor be responsible for both the manufacturing of the PC boards and the loading of its components.

In order to meet our aggressive schedule, we procured all electrical components in advance; the vendor was responsible for board procurement, nuts & bolts, loading, and flying-probe testing.

Since we need to deploy 98 systems, we planned for a full production of 100 boards, plus 25 spares. This process had no big surprises; the only problem was caused by damage to the filters in the output circuit, which were not sealed and were damaged in the cleaning process. This was discovered in a pre-production run, so for the final run we attached the filters to the board after the rest of the board was soldered and cleaned.

TEST STRATEGY

We approached testing in two phases. The first was in support of the development of the hardware and was aimed at maximizing performance and optimizing the design. The second is the ongoing acceptance testing of

the boards built in quantity. The most important performance measurements characterized channel cross-talk, digitizer noise, signal distortion and non-linear behavior.

System Testing

The input channels noise and crosstalk measurements are performed on the AFE and DFE combined, essentially using the FPGA and ADCs as a sampling scope, transmitting the raw data over the network connection, and analyzing the data at an ordinary workstation. Results are presented below.

Similarly, the DFE and RFO were used to perform linearity analyses, driving the output from the network connection through the FPGA.

The integrated system was measured for overall performance. Since the system is based on the VME/VXI form-factor, we compared the relevant measurements by testing the same hardware on the PCI platform used by the beam diagnostics group.

Acceptance Tests

Testing of the production hardware is being performed by testing the same functions and characterizing the each board either individually or as a subsystem. For example, the DFE and RFO are tested together, because there is no simpler way to feed high speed digital data into the RFO.

PERFORMANCE RESULTS AND MODIFICATIONS

One of the performance improvements we implemented in the testing phase was the adoption of a shield plane between the DFE+RFO and the VXI motherboard. Since our schedule did not allow us for further troubleshooting, this shield has effectively worked to limit the broadband noise from VXI bus transactions, which was seen in the 50 MHz output section, and then was mixed up to generate strange spurs in the RF band. The noise has recently greatly suppressed by modifying the FPGA firmware to allow for better routing of the output gates. This change might eliminate the need for the shield.

Modifications to the DFE

The differential clocks supplied to the AD6645 high speed ADC's needed careful attention, including last minute component changes, before the input ADC subsytem achieved the desired noise floor of -140 dBc/Hz. This signal comes from a low jitter differential LVPECL 80 MHz VCXO, divided by two, transformer coupled, and transmitted across approximately 12 cm of circuit board. Data-dependent noise is observed, presumably due to capacitive coupling from the ADC data lines to the clock traces. Figure 1 shows the effect, both before and after optimizing the clock trace drive circuitry, and a comparison with the interim system used as a benchmark.

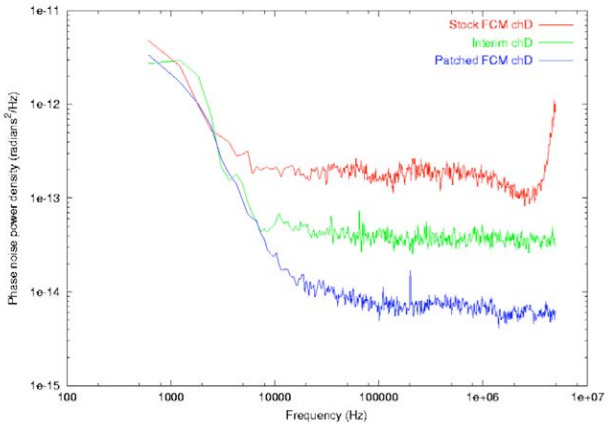

Figure 1: Clock circuit modifications on system noise.

An interesting byproduct of the noise measurements is the characterization of our signal sources. Since the noise measurements were made using various reference sources, we could extract their noise performance in our frequency range, and compare the $5 crystal with the $10,000+ signal generator or the SNS master oscillator. Needless to say, the crystal is second to none, as shown in Fig. 2.

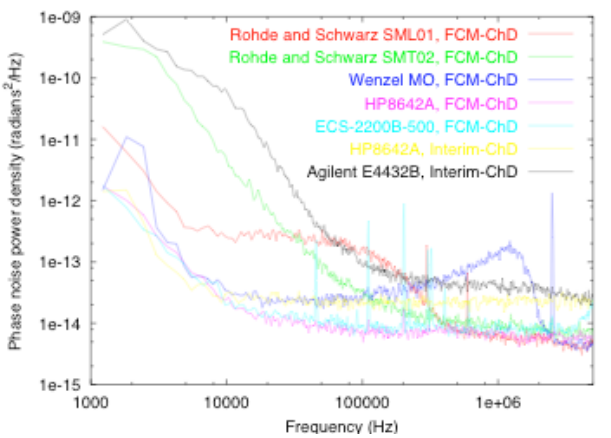

Figure 2: Phase noise comparison of several RF sources.

Results from Tests at SNS and Jab

The FCM operation was also thoroughly tested on the complete system. The results including klystron and RF cavities. The system closed loop performance already reached results well within the 1%, 1 deg. specification. While running standalone, the closed loop system demonstrated a stability of about 0.2% and 0.2 deg (Fig. 3), while during the last beam run the observed stability has been 0.5% and 0.5 deg. While these results were obtained with some effort to optimize performance, the system firmware is still under development. Improvements such as adaptive feed forward algorithms and shaping the turn-on curve are aimed at improving performance further. Such firmware will be available for operation with the SCL.

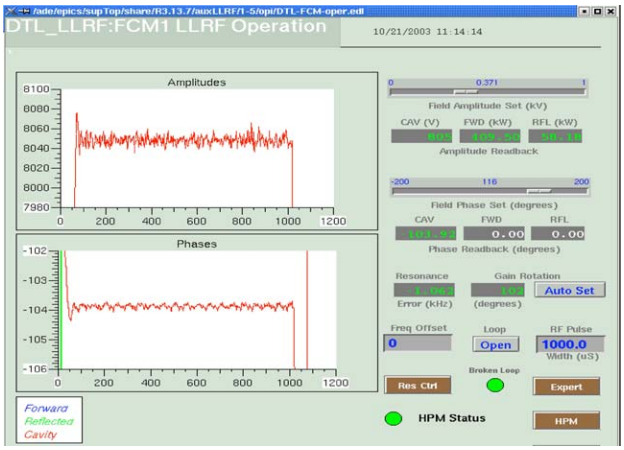

Figure 3: Test results on the DTL1 – amplitude and phase regulation to 0.2%, 0.2 deg.

Although these initial results are very encouraging, scaling these results to the large number of stations required for operation of the full linac will require adequate testing time and is certainly a challenging task.

FIRMWARE ARCHITECTURE

Since project inception, we have split tasks between firmware and controls software by assigning all actions taken within the pulse to the FPGA and those that are taken pulse-by-pulse to the software. For example, cavity tuning algorithms are implemented in software, whereas amplitude and phase feedback are a task of the firmware. The EPICS sequencer is now fully integrated in the operation of the system. The overall system architecture, which highlights the interaction between software and firmware, is shown in Fig. 4.

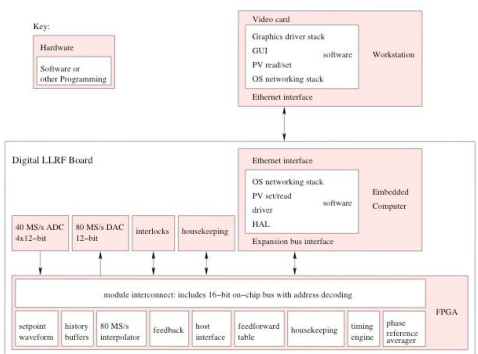

Figure 4: Software-firmware architecture.

Automated Code Generation

An important addition to the code set is that of the automated generation of a Verilog module to interconnect components: intercon.pl (241 non-blank, non-comment lines) creates a top level module to instantiate and interconnect second level modules, parse argument lists in Verilog modules, and build up the top-level Verilog program that instantiates each of them.

The intercon "framework", admittedly foreign to anyone browsing the code for the first time, is designed to minimize the amount of human-maintained overhead needed to support "real work" done in those second level modules. Along with the reduced line count should come reduced chances of introducing errors during maintenance of the code.

Each second level module defines its ports in a well defined manner, from the following categories: pins -- simply brought up as pins at the top level; interconnect -- like-named ports are interconnected to other second level modules, so the top level acts like a virtual backplane; host registers -- address ranges specified for read and/or write

PLANS FOR THE FUTURE

With the delivery of the production boards, we will be assembling and testing systems while supporting cavity installation and conditioning. A beam commissioning run is scheduled for September and it will include the linac up to the CCL system. This is the last scheduled beam run until the full linac commissioning in 2005. At this time, 35 LLRF systems have been installed in the klystron gallery.

The firmware development will continue throughout next year. While operation with superconducting cavities has been previously demonstrated, and the controller is used to condition cryomodules, a lot of development is still planned for the coming months. Lorentz force detuning and optimized turn on profiles will be studied and implemented, as well as a possible interface with a piezo-tuner controller. To further improve performance, we will also study and implement adaptive feed-forward algorithms. Auto-configuring routines will also be added to simplify settings of the linac for operator's control.

ACKNOWLEDGMENTS

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