# A HIGH-RESOLUTION S-BAND DOWN-CONVERTING DIGITAL PHASE DETECTOR FOR SASE FEL USE

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*Abstract*

Each of the rf phase detectors in the Advanced Photon Source linac [1] consists of a module that down converts from S-band to 20 MHz followed by an analog I/Q detector. Phase is calculated from one digitized sample per pulse each of I and Q. The resulting data have excellent long-term stability but are noisy enough so that a number of samples must be averaged to get a usable reading. The more recent requirement to support a self-amplified spontaneous emission (SASE) free-electron laser (FEL) has presented the need to accurately resolve the relative phase of a single pulse. We replaced analog detection with digital sampling and replaced internal intermediate frequency (IF) reference oscillators with a lower-noise external oscillator in order to control the two largest components of noise. The implementation of a central, ultra-low-noise reference oscillator and a distribution system capable of maintaining the low phase noise is described, together with the results obtained to date. The principal remaining technical issue is determining the processing power required as a function of measurement channels per processor, measured pulse repetition rate, intrapulse data bandwidth, and digital filter characteristics. The options and tradeoffs involved and the present status are discussed.

## DEFINITION OF PROBLEM

### *Existing System and Limitations*

The existing LANL-designed linac phase detectors utilize down conversion from 2856 MHz to 20 MHz (Downconverter VXI Module), followed by ovenized analog I and Q detectors that produce one 12-bit digitized sample per pulse for each of the I and Q waveforms (Vector Detector 2 slot VXI module). Software in the input/output controller (IOC) performs a rectangular-to-polar conversion on the data samples, extracting phase and suppressing amplitude. Excellent long-term stability has been achieved. However, these detectors have exhibited over one degree of noise on the measurement.

### *Requirements for Improved Performance*

The more recent requirement to support a SASE FEL [2] has presented the need to accurately resolve the relative phase of a single pulse. The following requirements have been determined as goals for upgrade efforts.

- Compatibility with existing, VXI-based, down-converting (to 20 MHz) hardware
- Resolution of $\leq 0.1$ degree rms based on single-pulse data (without averaging multiple pulses)
- Capability of supporting up to four measurements/subsystem in the operational environment
- Operational Environment:

| | |
|---|---|
| Pulse rep. freq. | 30 Hz max |
| Sampled pulse width | 1.3 µs max |
| Intrapulse data bandwidth | 10 MHz |

## DIGITAL CONCEPT AND EXPERIMENTS

An internal APS presentation [3] identified phase detection as one of a number of applications that could potentially benefit from cost-effective performance improvements associated with the use of digital signal processing (DSP).

In order to maximize the pulse envelope bandwidth, the existing design employs minimal filtering of the IF carrier. DSP easily incorporates high performance filters that could reduce carrier noise. Newly announced sampling modules using state-of-the-art flash analog-to-digital converters that could support the desired 80-MHz sampling rate were identified. DSP would allow acquisition of the phase waveform of the portion of interest of a complete pulse, which could then be averaged in different ways for different purposes. For instance, one point in a pulse could be averaged over a number of pulses to get an extremely steady phase value for screen display and long-term auto phase correction. At the same time, the entire portion of interest of a pulse could be averaged into a composite phase value, which would have low enough effective noise to be effectively compared with the equivalent value for an adjacent pulse.

A frequency quadrupler was constructed and experiments were performed comparing digital sampling to the existing analog system. A key finding from the initial experiments was that the phase noise of the 20-MHz IF reference oscillator, used by the Downconverter Module, constitutes the most critical limitation that constrains the phase measurement performance. This implementation is especially sensitive since the approximately 143X down conversion adds phase noise that is 43 dB greater than the reference oscillator phase noise to both the down-converted signal and the down-converted 2856-MHz reference. Furthermore, the digitally sampled data is degraded even more than the analog data when the noise level is as great as that of the existing system.

## ULTRA-LOW-NOISE OSCILLATOR

An ultra-low-noise oscillator, from the Wenzel Associates ULN series, has been procured. This oscillator

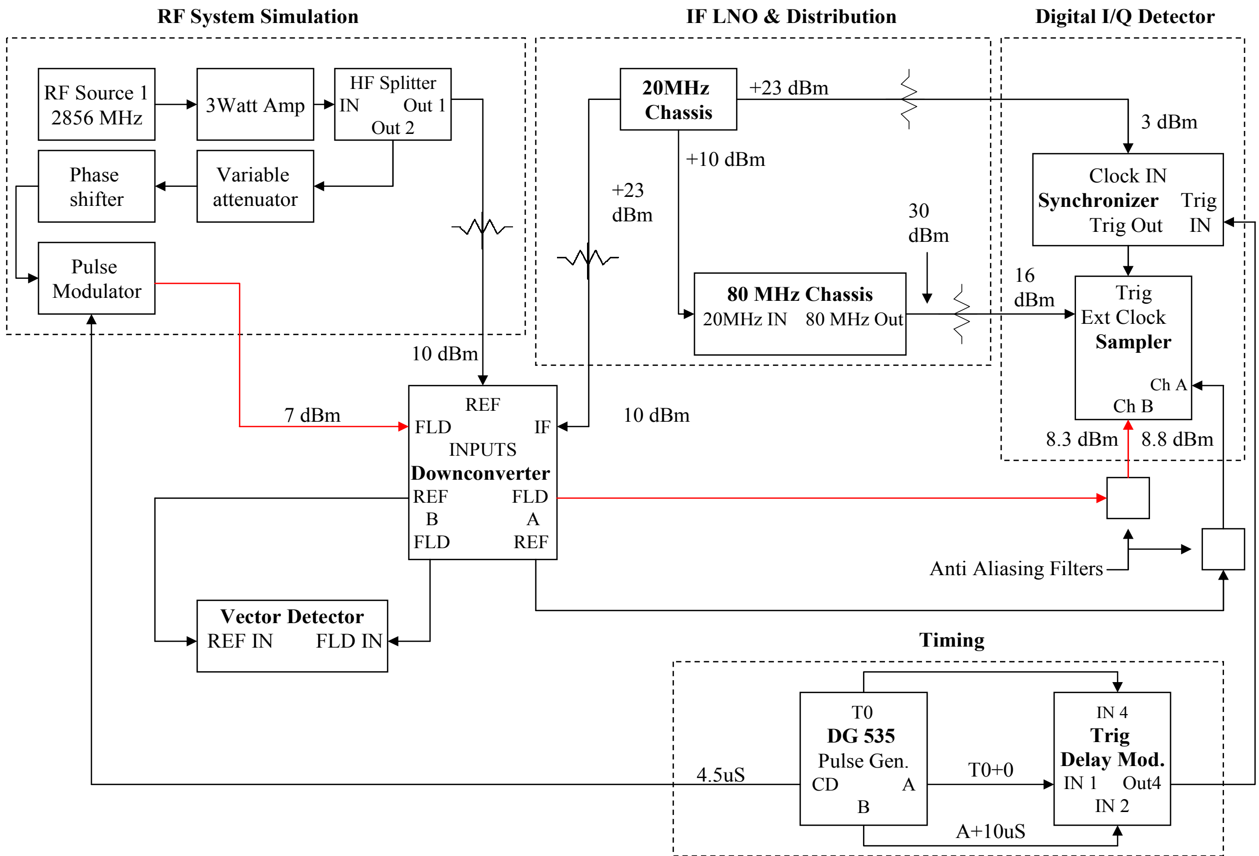


Figure 1: Phase detector comparative test configuration.

has phase noise specifications 30 dB below those of the 20-MHz IF reference oscillator that is internal to the Downconverter Module. A revised topology that replaces the internal reference oscillator with the ultra-low-noise oscillator as an external 20-MHz reference was tested. The results show that when the phase noise of the 20-MHz source is low enough, the digital phase measurement has a lower noise level than the analog. This is as expected, since carrier noise is lower. Figure 1 shows the most current version of the test configuration.

## CENTRALIZED 20 MHZ AND 80 MHZ

### *Distribution Concept*

There are seven IOCs supporting rf measurements in the Advanced Photon Source linac. The size and cost of the ultra-low-noise oscillator are both beyond comfortable limits for incorporation within a VXI module. The use of a centralized subsystem, incorporating the ultra-low-noise oscillator and the quadrupler, together with amplification and 8-way fan-out, was chosen as a cost-effective way to obtain the two required frequencies with the necessary low phase-noise characteristics.

### *Distribution Implementation*

A key design issue was avoiding phase-noise degradation in amplifying 20 MHz. The precise noise figure of the amplifier is not critical. However, excellent effective linearity is required in order to minimize AM-to-PM conversion. The amplifier configuration selected uses an amplifier incorporating feedback with gain limited to 15 dB, followed by a phase-optimized bandpass filter having 35% band width. This identical configuration is used both before and after an 8-way splitter. Maximum power output is limited to 10 dB below typical 1-dB compression power. This configuration produces test results indistinguishable from those obtained by using the unamplified oscillator as the down-conversion reference.

The centrally distributed 20-MHz and 80-MHz subsystem has been implemented in the form of separate 20-MHz and 80-MHz chassis, which have been installed in a central location in the linac, plus Dual Distribution panels/chassis at each IOC. Each Dual Distribution panel/chassis provides eight 20-MHz jacks and four 80-MHz jacks. This subsystem has been made active as the IF reference for the Downconverter Modules. The additional 20-MHz and 80-MHz outputs that have been provided will support experimental and, later, operational digital phase detectors that will eventually supersede the Vector Detector Modules.

## PROCESSOR CONSIDERATIONS

Processing requirements are minimized by the use of the 4X oversampling since the I/Q calculations require no multiplications (sin/cos of 0, 90, 180 and 270 degrees are -1, 0, +1). An MVME5100 processor is already in use at the APS and is expected to have adequate performance.

## TEST RESULTS

Figure 2 shows stability test results with and without an anti-aliasing filter having a 3-dB bandwidth of 55 MHz.

## OPTIONS AND TRADE OFFS

The results to date appear to meet the requirements of the application with a performance margin. Most of the data points are less than 0.07 degrees. This approach is preferred because it maintains compatibility with the existing hardware.

However, the true optimum calls for choice of a higher IF. Oscillators from the Wenzel Associates ULN series are available at higher frequencies, including 100 MHz. The lesser down conversion will result in a 14-dB decrease in noise on the down-converted signal. This is offset by a 5-dB increase in specified noise in the higher frequency oscillators, resulting in a 9-dB net improvement. The effective net improvement can be expected to be 7 dB after subtracting a 2-dB improvement from the anti-aliasing filter, which probably would not be practical for that case, meaning that most data points will be less than 0.03 degrees, i.e., a time uncertainty of 30 fs.

On the other hand, optimum performance versus total cost from scratch is likely to be produced by direct digital sampling. In this case, the aperture uncertainty of the analog-to-digital converter is the principal error. Aperture uncertainty of 100 fs is currently available

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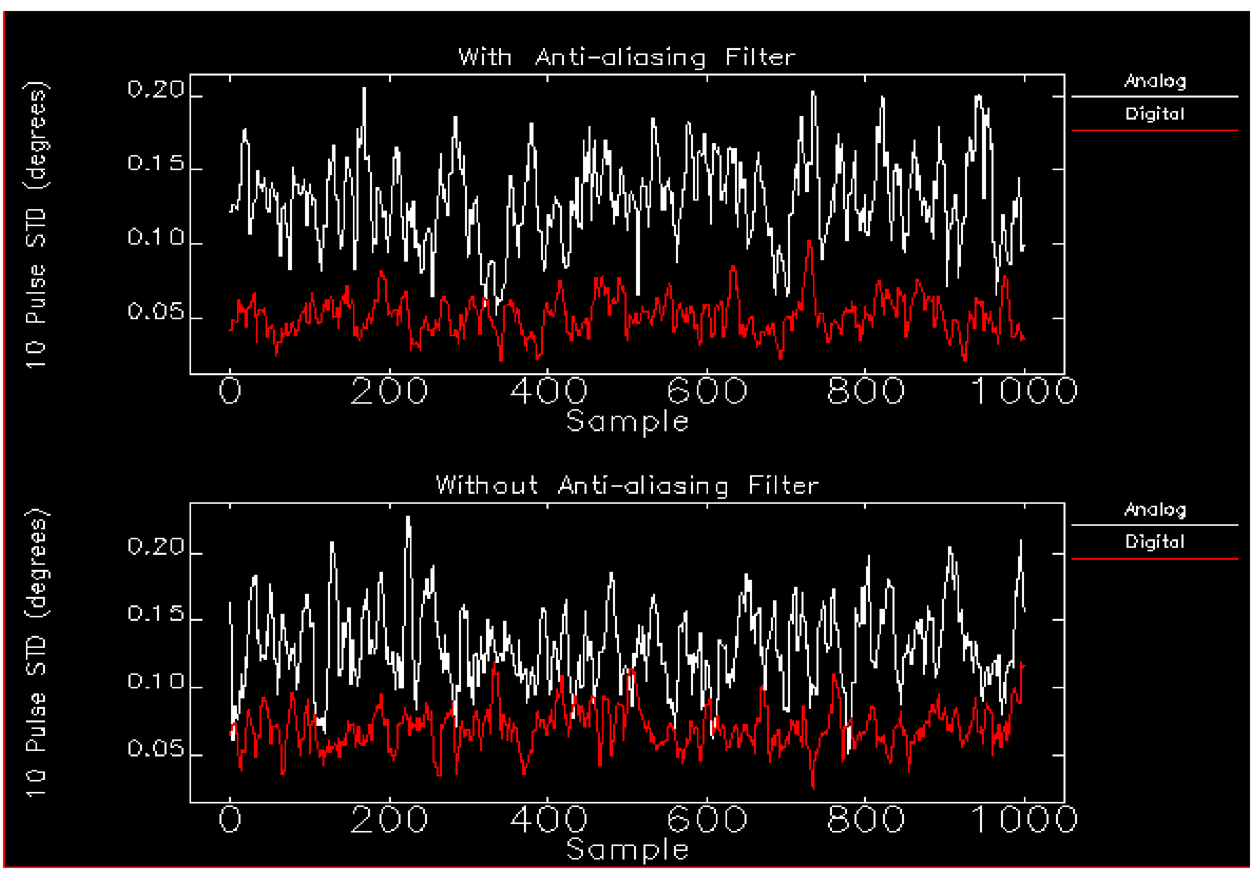


Figure 2: Comparative stability test results.