THE RF-STATION INTERLOCK FOR THE EUROPEAN X-RAY LASER

T. Grevsmühl, S. Choroba, P. Duval, O. Hensler, J. Kahl, F.-R. Kaiser, A. Kretzschmann, H. Leich, K. Rehlich, U.Schwendicke, S. Simrock, S. Weisse, R. Wenndorff, DESY, Germany

Abstract

The RF-station interlock for the European X-ray laser will be based on a 19"- 3U crate incorporating a controller with the 32-bit RISC NIOS-processor (ALTERA). The main task of the interlock system is to guarantee safety of personnel and prevent any damage from the components of the RF station and connected cavities. The interlock system must also guarantee a maximum time of operation of the RF stations which implies the implementation of self diagnostics and repair strategies on a module basis. Additional tasks are: collection and temporary storage of status information of the individual channels of the interlock system, transfer of this information to the control system, slow control functions (e.g. HV setting and monitoring) and control of inputs and outputs from and to other subsystems. In this paper we present the implementation using an ALTERA-FPGA running a 32-bit RISC NIOS-processor. Connection to the accelerator main control is provided by Ethernet using BSD-style socket routines based on ALTERA's plugs-library. The layout of the system is presented and first hardware components are shown.

INTRODUCTION

The RF system for the European XFEL consists of 35 RF stations supplying RF power at 1.3GHz for the superconducting cavities of the linear accelerator of the XFEL [1]. Each RF station generates RF pulses up to 10MW at a pulse duration up to 1.5ms and a repetition rate up to 10Hz. A station consists of a klystron, pulse transformer, pulsed high voltage power supply, a low level RF system, auxiliary power supplies and an interlock system [2]. A simplified view is shown Figure 1. The pulsed high voltage power supplies will be installed in a separate hall above ground whereas all other components will be installed in the accelerator tunnel under ground near to the cavities. Connection between the components in the hall and in the tunnel is accomplished by high voltage pulse cables and control and interlock connections. The main task of the interlock system is the protection of the different subsystems of the RF stations and of the components connected to the station. In addition it provides slow control functions for the subsystems. Since the interlock system is installed in the accelerator tunnel, where no access is allowed during beam operation, the interlock system has to provide monitoring functions, allowing the localization of failures of the RF station remotely which sets the service personnel in a position to exchange broken subunits quickly during a scheduled maintenance time. In addition all monitored signals will be transferred to the accelerator main control system, where correlations between accelerator and RF station operation can be determined. The interlock system is a modular system so that malfunctioning interlock boards can be exchanged without renewing a complete system.

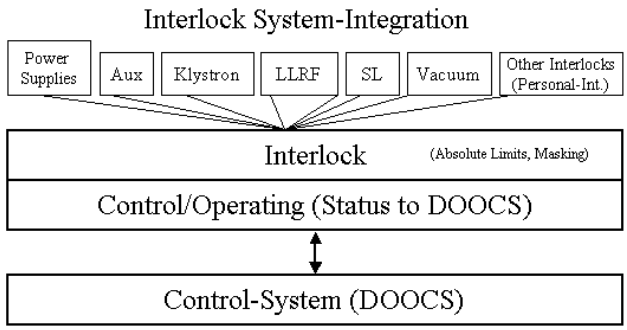

Figure 1 : RF-Station components (simplified).

REQUIREMENTS

To serve its main task the interlock system has to deal with 3 types of errors:

-hard component failures (non-reversible hardware mal-function like broken cables, damaged contacts, dead sensors, ...)
-soft errors (e.g. sparks in the klystron or wave guide system, temperature above a threshold, water-flow...)
-error conditions caused by transient noise from the RF station itself (caused by the pulsed power operation)

Errors should be treated with two types of thresholds and channel masking.

Absolute max./min. thresholds: any violation of these thresholds will force the shutdown of one ore more subsystems or of all components of the RF station.

Programmable (soft) thresholds: a violation of these boundaries will generate an alarm message to the control system. Soft thresholds are only available for analog input channels.

For any individual input channel a mask function should be implemented which allows to exclude this channel from all of the interlock functions. Masking operations via the control system are secured by password mechanism and must cause an entry into a log file [3,4].

Besides additional tasks like setting operational parameters, collecting status and diagnostic information and providing it to the main control system, a system self test at power-up has to ensure the proper operation of all interlock components. This is also true for a test during normal operation. In case of power-down status-information should be saved for diagnostics. The RF-

station interlock has to interact with other XFEL-subsystems (see Figure 2).

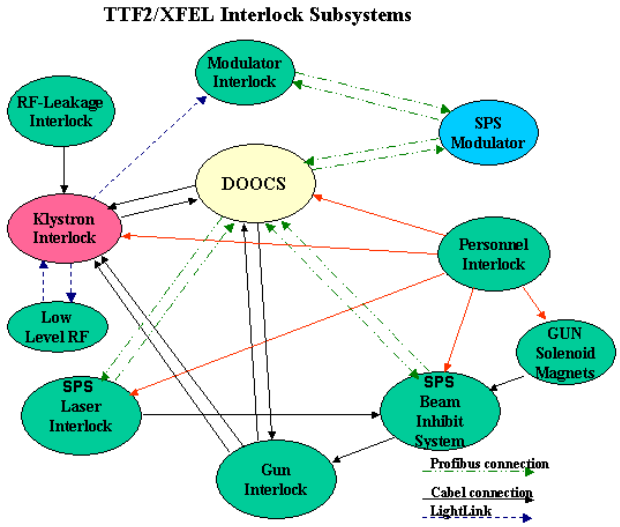

Figure 2 : Interaction of different XFEL-subsystems.

Other implementation constraints are :

- process-I/O should not use cables to/from the front side of the crate; all cabling must be done from rear site
- due to the future XFEL-tunnel layout a space saving implementation of the system is needed e.g. a combination of all interlock functions and some slow control functions into only one crate per RF-station
- perform communication between modules via a backplane (no extra cables for communication)
- connection to the main control system DOOCS via ethernet

IMPLEMENTATION

The interlock mechanics is a 19" 4U crate with dedicated backplane optimized to the application (figure 3, 4, 8).

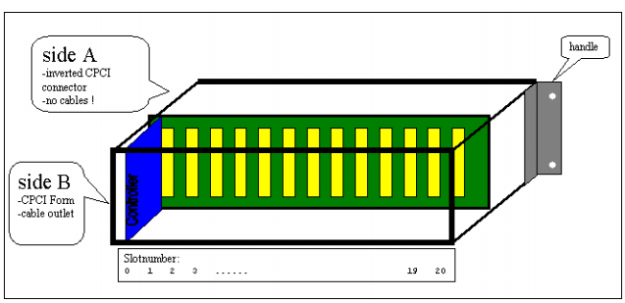

Figure 3: Interlock Crate Layout.

A 3U cPCI-like board format with two 5-row connectors is used (figure 5). 235 pins to the backplane per board give enough pin resources per slot and to the backplane to build a compact interlock/control system.

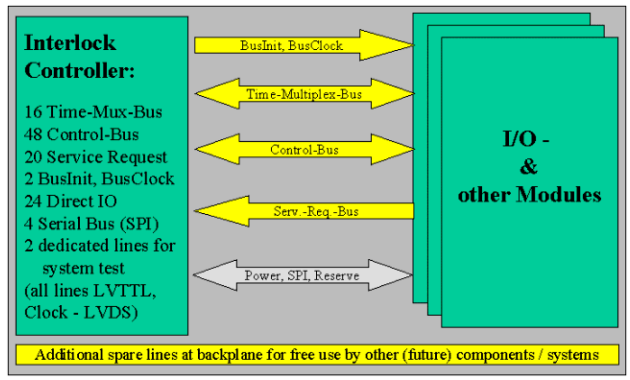

Figure 4: Dedicated Backplane Layout.

Figure 5: Interlock Controller.

Each interlock system consists of 1 controller and up to 20 I/O-modules (figure6).

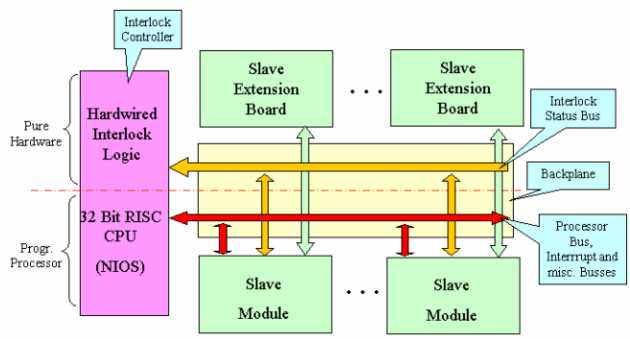

Figure 6: Interlock System Layout.

At the interlock controller board an ALTERA FPGA, a Cyclone EP1C20F400-C7 FPGA is used (figure 5, 7). Inside the FPGA the following is implemented:

- interlock function for components of one RF station based on signals pre-processed within the different IO-modules
- interface to the DOOCS control system via ethernet
- controls of the IO-modules in the crate
- master of all backplane busses
- source of the bus timing signals
- some slow control functions
- system check after power up or per command

All necessary control functions to all slave modules in the interlock crate and the interfacing to the control system are performed by a 32-bit RISC NIOS CPU inside the FPGA. It is important to recognize that the interlock functionality inside the FPGA is strictly separated from software running at the NIOS CPU. The interlock will always work independently from the state of the CPU (figure 6, 7).

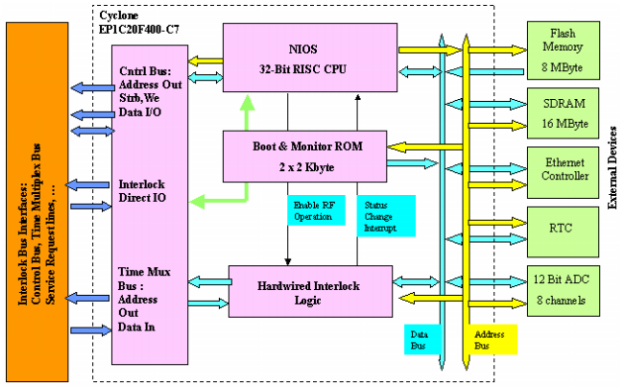

Figure 7: Interlock Controller Board Layout.

A TINE[5] server will run on the NIOS CPU and will provide the interface to DOOCS clients via Ethernet. The following is transmitted via the interface: status information, mask data, current values of analog input channels. Commands will also be available in the control system as properties, whose settings along with all other information will be made available in the DOOCS History Format.

The TINE kernel relies on BSD sockets and must somehow be interfaced to the ALTERA-FPGA plugs library. To this end, a BSD-style socket library, based on ALTERA's plugs-library, supporting UDP, TCP, and standard BSD-routines, was developed, allowing a seamless integration of the TINE kernel. This approach has decided advantages as many more NIOS-compatible ALTERA devices (irrespective of NIOS II) are supported and no additional license is needed for the upcoming NIOS II. Due to the small-footprint of the TINE NIOS kernel one can run a standard TINE FEC, as is used at the DESY accelerators, directly on an ALTERA device! Standard network protocols can be used and very compact FEC-designs are possible.

RESULTS

Several hardware components and the TINE NIOS kernel are available and tested. Parts of the design used in the actual interlock hardware at TTF2 show the stability and the reliability of the components. More IO-modules and the software for the interface to the control system are under construction. Options for the remote reconfiguration of the FPGA's are being investigated.

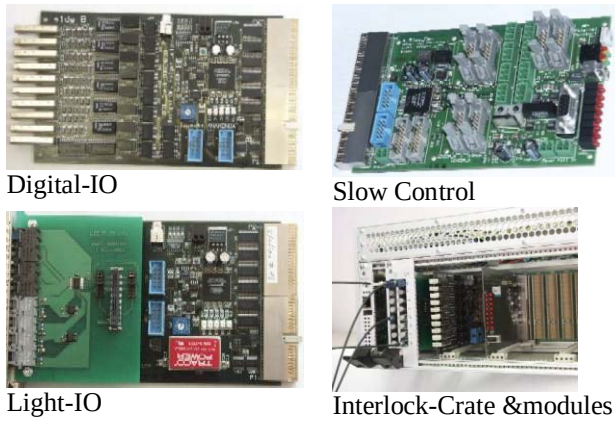

Figure 8: Hardware parts of interlock system.

CONCLUSION

A very compact, scalable interlock system for the XFEL-RF-stations has been designed and partly tested. It uses an ALTERA-FPGA running a 32-bit RISC NIOS CPU with a BSD-style socket library plus TINE kernel. The layout of the system is now almost completed. Prototypes with limited performance have been built and are in operation at the new RF stations of the DESY VUV-FEL (Tesla Test Facility). It is planned to install extended versions of these prototypes in the older VUV-FEL RF stations when the next generation of boards are available.

REFERENCES

[1] TESLA Technical Design Report, DESY TESLA-2001-011, 2001
[2] S. Choroba, The TESLA RF System, in High Energy and High Power RF, Proceedings of the 6th Workshop on High Energy Density and High Power RF, Berkeley Springs, West Virginia, 22-26 June 2003, AIP Conference Proceedings, Vol. 691, P. 1-14
[3] S. Choroba, T. Grevsmuehl, H. Leich, S. Simrock, "The TTF2 / XFEL Klystron Interlock: Requirements and Implementation" (Requirements_Draft.doc)
[4] H. Leich, Report at Spring Conference of the SEI, (SEI_290304.ppt)
[5] http://desyntwww.desy.de/tine