

CONCEPTUAL LLRF DESIGN FOR THE EUROPEAN XFEL

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Abstract

The LLRF System for the superconducting cavities of the European X-FEL must support amplitude and phase stability of the accelerating fields of up to 0.01% and 0.01 deg. respectively. The stability must be achieved in pulsed operation with one klystron driving 32 cavities. This goal can only be achieved with low noise downconverters for field detection, high gain feedback loops and sophisticated feedforward techniques. State-of-the art technology including analog multipliers for downconversion, 100 MHz ADCs with high resolution up to 16 bit, and high performance data processing with FPGAs with a few hundred nanosecond latency allow to meet these goals. The large number of more than 100 input channels (including probe, forward and reflected signal of each of the 32 cavities) and more than 34 output channels combined with the tremendous processing power requires a distributed architecture using Gigalink interfaces for low latency data exchange.

INTRODUCTION

The LLRF System, accelerator instrumentation, and control system constitutes a significant of electronics in the XFEL tunnel. The operational goal of more 90% uptime imposes an availability of more than 99% on the llrf system which is unachievable with current approaches considering that the tunnel is only accessible during one short maintenance period per month. The design must be fault tolerant to avoid interruptions in operation due to single-point failures. This presents both a hardware and a software challenge, as well as a severe challenge to design for cost as well as HA. Industrial standard solutions are preferred which leads to the choice of ATCA and uTCA as an attractive alternative to the presently VME and cPCI standard.

Other criteria for the choice of standard are the desire for modularity which allows to combine several boards with different functionality to the desired system. This will simplify maintenance and reduce maintenance cost. Fast Gigabit communication links between the boards within a crate and between crates are required to support low latency real time feedback systems and transfer of large amounts of data between systems.

Other considerations include scalability, maintainability, and remote diagnostics. Since the hardware is a major investment and cannot be replaced frequently, it must support future hardware and software upgrades. This means that spare IO channel and adequate computational capacity must be included in the original design.

HARDWARE ARCHITECTURE

The rf control system for one rf station consisting of a 10 MW klystron driving 32 cavities in 4 cryomodules must provide control of the vector-sum of all cavities with a stability of the order of $2e-4$ for amplitude and up to 0.01 deg. in phase at 1.3 GHz. The feedback system requires individual field measurements from which the vector-sum is calculated as well as forward and reflected power measurements from which cavity detuning and beam phase are derived and which are used for system diagnostics. To support a low latency in the feedback loop of less than 1 μ s, 100 MHz ADCs with 14-bit resolution and DACs both with few cycle conversion times as well as a low latency processing unit based on large FPGAs are required. The field detection is accomplished by downconversion of the cavity probe signal at 1.3 GHz to an IF frequency of about 50 MHz which is sampled by the ADC from which the field vector is calculated. A vector-modulator driven by a DAC allows fast control of the incident power in amplitude and phase. Piezotuner support fast cavity tuning to compensate Lorentz force detuning.

The proposed architecture for the LLRF system is shown in figure 1. Crates (possibly uTCA) placed close to the cryomodules accommodate field detection boards with downconverters, ADCs and FPGA for processing the partial vector-sum of 8 cavities. The same boards are also used for the measurement of forward and reflected power. The boards are connected by low latency links to allow for real time algorithms which calculate cavity detuning, beam phase and other derived measurements required as input for various algorithms. Also installed in this crate is a processor board which takes care of the shelf management and can be used to implement a control system front end server supplying the necessary parameters to the individual boards. A timing receiver provides event triggers and clocks necessary for operation. Piezo drivers allow fast control of the cavity resonance frequency using piezo actuators for control.

In the center of the 32 cavity section is a shielded area for the racks which house the main control electronics. A control system crate (possibly ATCA) accommodates a processor board with FPGAs and DSPs in which the main rf control algorithms are implemented. Low latency fiber optic links are used to send the data from the front-end crate to the main processor board.

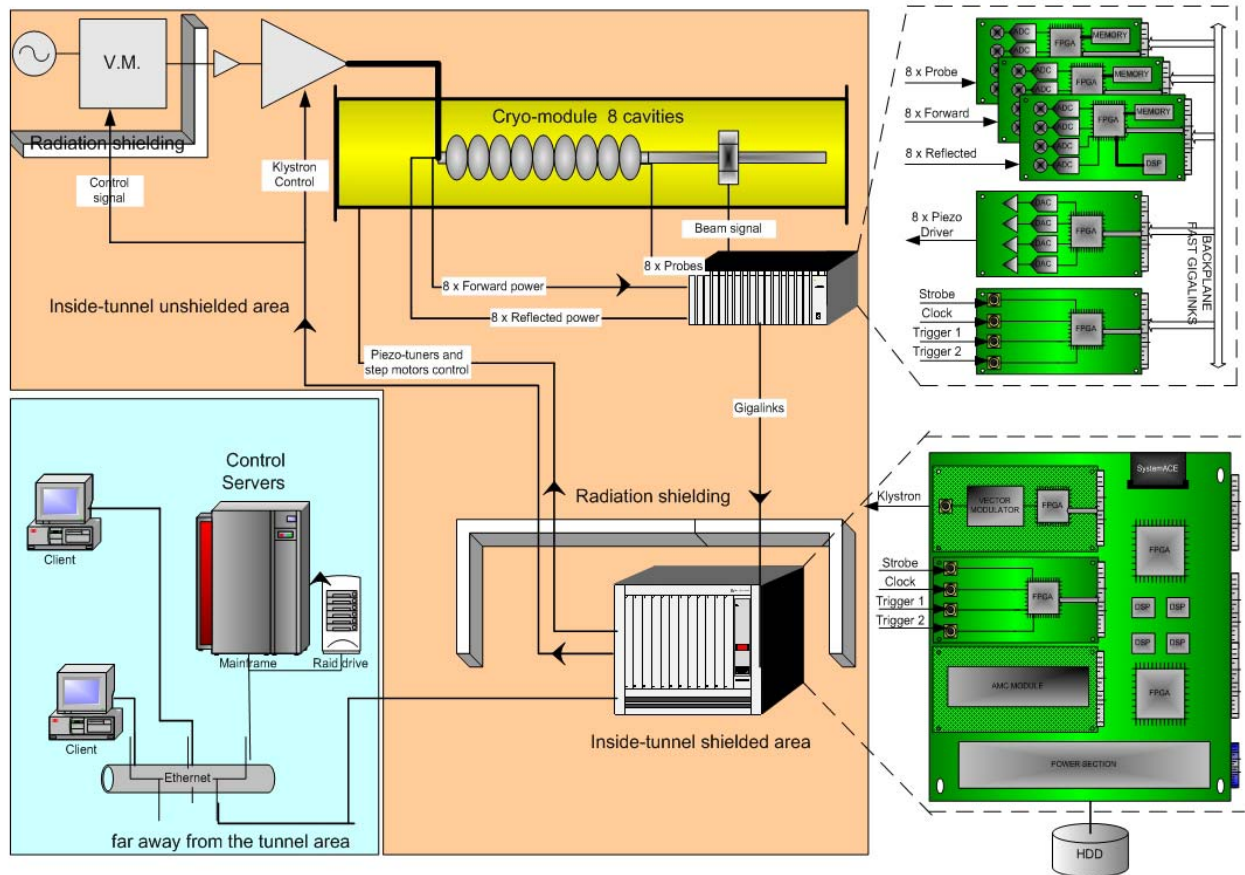


Figure 1: Hardware architecture for the LLRF system.

The middle layer server and client computers are installed in the service buildings and control room. Here implements are the servers for automation of operation and the clients providing the interface for the operators.

The frequency and timing distribution system will deliver reference phase, event triggers and clocks to all crate locations. Calibration signals are available at the downconverters to ensure long term phase stability.

SOFTWARE ARCHITECTURE

The software implementation of the rf control system must also support high availability including:

- low latency algorithms
- distributed algorithms
- modularity of algorithms (interface !)
- exception handling
- build-in diagnostics
- beam based feedback
- remote control
- redundancy
- data storage
- SEU immunity

The low latency in the feedback algorithm is supported by the massive parallel processing in the FPGAs. However the algorithm must be kept simple to achieve it goal. Complex algorithms requiring floating point calculations

such as adaptive feedforward, system identification and piezo tuner control can be implemented on floating point DSP processors since the latency requirements are not as stringent. The server for automation of operation can be implemented on a middle layer server CPU since the timing requirements are not as critical.

The distribution of the modular algorithms requires well defined interfaces to ensure simplicity in trouble shooting, maintainability, and upgradeability. Low latency links will use in-house protocols while commercial links protocols are available for links with high bandwidth which do not require the low latency. It will be challenging to distribute the algorithms on the various processing platform since detailed specifications are not yet available and depend also on the available allocation of resources. For fast global feedback algorithm including beam based feedback, the number of analog and digital IO channels must also be determined.

Redundancy can be achieved with algorithms which provide the same results from other signal sources. It is for example possible to calculate the cavity field from forward and reflected power although the measurement error is larger. Any discrepancy between the independent derived signals will flag potential errors in hardware or algorithms.

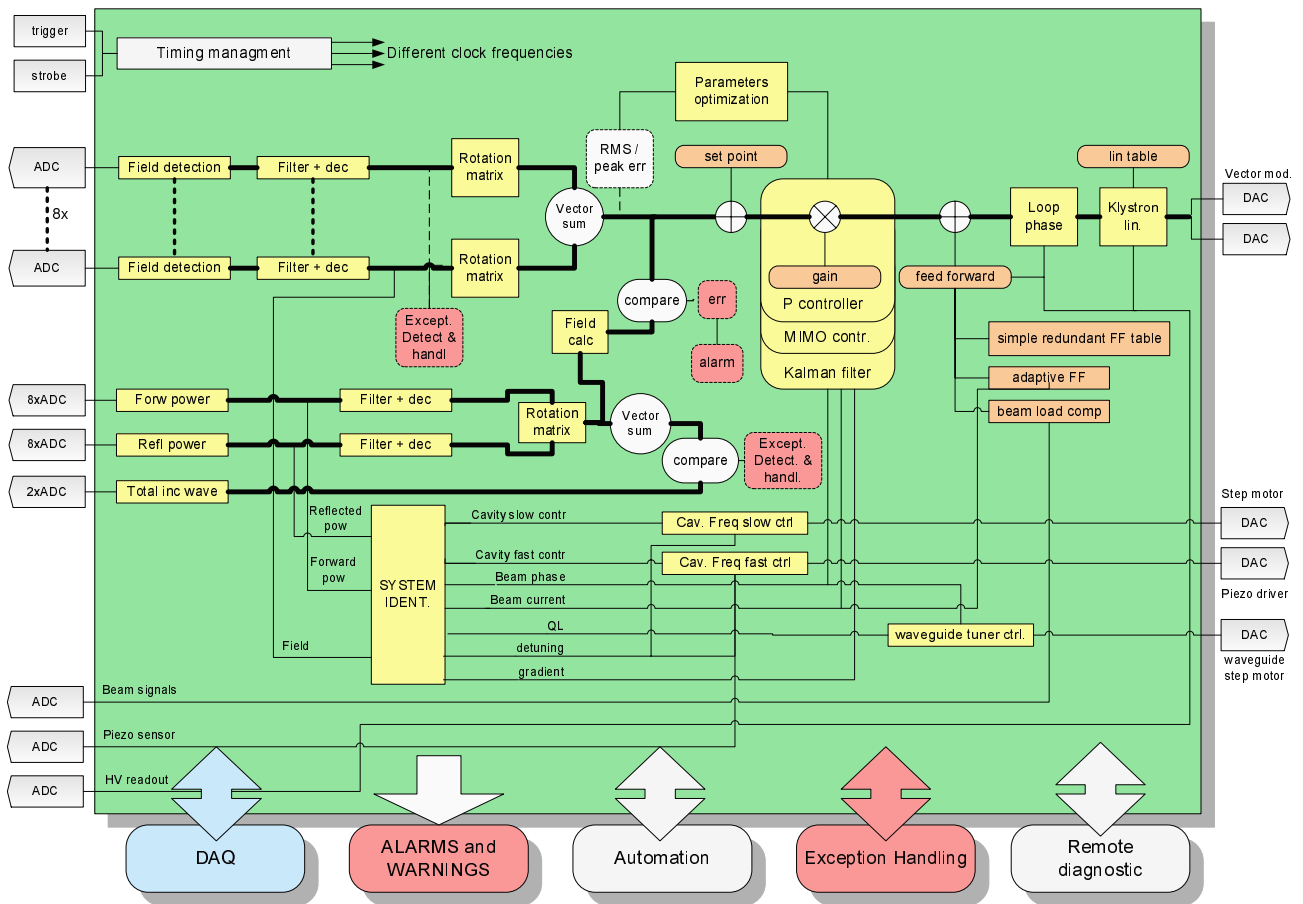


Figure 2: Architecture of the LLRF software.

Data storage is provided locally on most processor boards and will be distributed to the central servers between pulses for further signal processing.

Single event up-set immunity can be achieved by triple modular redundancy (TMR) methods which will be used only in small sections of the hardware. This part of the electronics is responsible to check for signal integrity and switch to the redundant feedforward if necessary.

Automation of operation will be essential for the control of almost 1000 cavities to ensure simplicity of operation and high availability. Therefore the front end hardware and software must support all features required for automation. Examples are measurement and setting of the following quantities:

- Field vector measurement
- Loop phase and loop gain
- Loaded Q and cavity detuning
- Beam phase and beam induced voltage
- Calibration of cavity field and phase
- Vector-sum calibration
- Calibration of forward and reflected wave
- Beam loading compensation (current and phase)
- Klystron linearization
- Exception detection and handling
- rms field errors
- warnings and alarms

It is desirable to implement the algorithms as close as possible to the hardware to reduce network traffic. However often it is more convenient to implement algorithms and applications at middle layer server or as client applications simplify the programming (in C or ++) and later upgrades as well as maintainability. Also good documentation is essential to achieve these goals and support the exchange of algorithm within collaborations. The tools for software development should be standardized to facilitate the exchange of software.

For the algorithm and application development it is important to define signals, algorithms and interface in an early stage so that the work can be distributed in modules to the different groups working on the implementation. For example it will be possible to implements procedures for automation if the interfaces and available signals are known well in advance.

CONCLUSION

The experience at FLASH and other accelerators has lead to a concept for high availability which is adequate for operation of electronics in a single tunnel in presence of moderate radiation levels. The modular concept using industrial standards permits future hardware and software upgrades. High level applications, exception handling, and build-in diagnostics will ensure the required high availability.