LOW-LEVEL RF SYSTEM FOR STF

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Abstract

The Super-conducting RF Test Facility (STF) has been constructed to establish the production technique of a cavity having a high gradient and operated for the high-power testing of the klystron and couplers being installed in the superconducting cavities.

An accelerating electric field stability of 0.3% (rms) in amplitude and 0.3 degree (rms) in phase is also required for the RF system in STF. In order to satisfy these requirements, a digital LLRF control system using FPGA is adopted, and the components required for the digital LLRF system have been developed.

INTRODUCTION

The Super-conducting RF Test Facility (STF) has been constructed to contribute to the International Linear Collider (ILC) project from FY 2005 at KEK. This STF includes two plans: Phase-I and Phase-II. In the Phase-I project, one 1300 MHz klystron is to deliver its RF power to two types of super-conducting cavities, one having a 35 MV/m gradient and the other a 45 MV/m gradient, for establishing the production technique of a cavity having a high gradient. STF Phase-I will be operated from FY2007 [1][2].

In STF Phase-I, an accelerating electric field stability of 0.3% (rms) in amplitude and 0.3 degree (rms) in phase is also required for the RF system. In order to accomplish these requirements, a low-level RF (LLRF) system including digital feedback control is adopted for flexibility of the feedback and feedforward algorithm implementation.

LLRF SYSTEM FOR STF

The LLRF system in STF has been developed based on the LLRF system in J-PARC [3]. A block diagram of the LLRF system for the klystron station is shown in Figure 1. The required fundamental components for the LLRF system are: 1) programmable logic controller (PLC) for the LLRF system, 2) generation of the accelerating RF (1300MHz) and clock (10 MHz, 40 MHz, and 1310 MHz) signals phase-locked with a 10 MHz reference signal, 3) cavity field control (Digital Feedback), 4) high-power protection and RF monitor, 5) klystron drive (Analog FB, 20dB and 400W amplifier). All of the components for the LLRF system are installed in two 19 inch standard racks.

The LLRF system, except for the digital feedback control units, has been operated for high-power testing of the klystron (TH2104A) and couplers being installed in the superconducting cavities. During operation of this high-power test, the maximum output power of the klystron was about 2 MW.

In the case of an RF discharge, the Fast Interlock module shut off the RF drive to the klystron within a few μs to protect the high-power components.

DIGITAL LLRF CONTROL SYSTEM

In order to accomplish the requirement of an accelerating electric field of 0.3% (rms) in amplitude and 0.3 degree (rms) in phase for STF Phase-I, we have been developing a control system that adopts feedback and feedforward control using digital signal processing (digital LLRF system). The digital LLRF system of STF

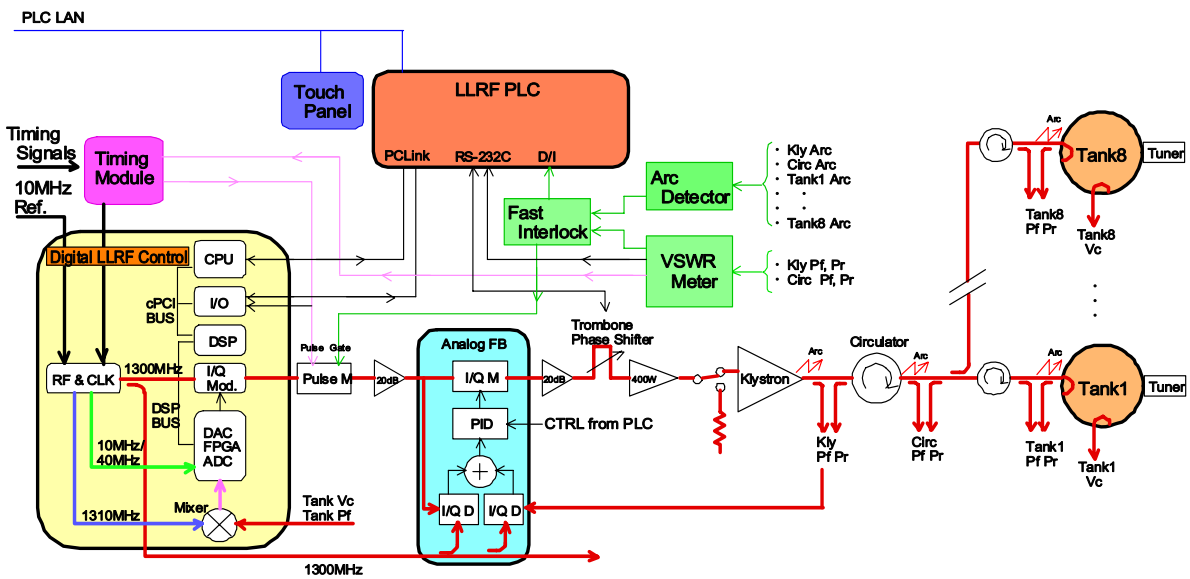

Figure 1: Block diagram of the LLRF system for STF.

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is comprised of a digital part and an analog part, as shown in Figure 2. The digital part consists of CPU, DSP and I/O boards installed in a compact PCI (cPCI rack) and one mezzanine board (FPGA) installed on the DSP board. The analog part is composed of RF&CLK and Mixer&IQmod units.

In the digital LLRF system for STF Phase-I, the FPGA board, the RF&CLK unit and the Mixer&IQmod unit have been newly developed based on the digital LLRF system for J-PARC [4].

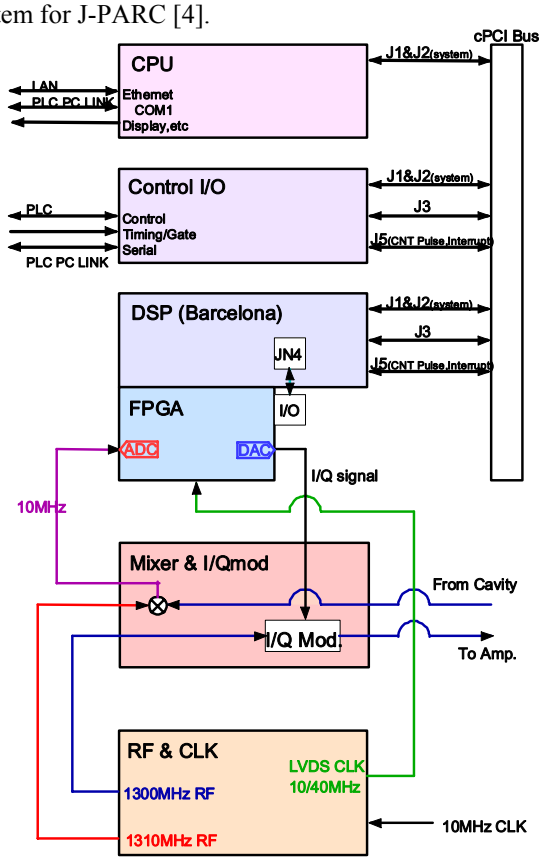

Figure 2: Block diagram of the digital LLRF control system for STF.

RF&CLK Unit

The RF&CLK (RF and clock generator) unit receives a 10 MHz signal from a master oscillator, and creates two timing clocks (10 MHz, 40 MHz) and two RF (1310 MHz 1300 MHz) signals synchronized with a 10 MHz external' reference signal, as shown in Table 1. In order to decrease the influence of the timing jitter caused by noise, the timing clock is outputted with the LVDS standard.

Table 1: Output signals of the RF&CLK unit

Freq. [MHz]	Signal	To
1310	RF	LO signal for Mixer
1300	RF	Input signal to I/Q mod.
40	LVDS	FPGA board
10	LVDS	FPGA board

The output phase noise of each frequency in the RF&CLK unit was measured with the E5052A from Agilent; the spectrum of phase noise in the RF signal of 1300 MHz is shown in Figure 3.

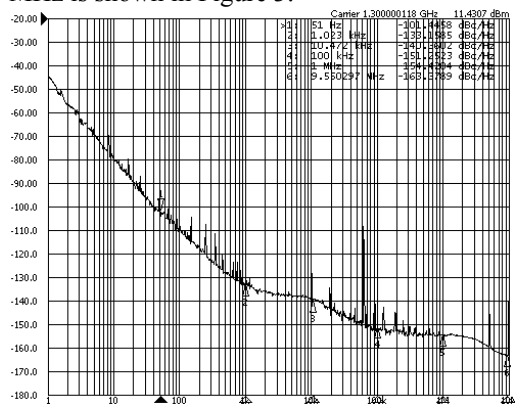

Figure 3: Phase noise of 1300 MHz RF signal.

In Figure 3, the horizontal scale is the offset frequency and the vertical scale is the SSB phase noise in dBc/Hz. The result of the rms phase noise is estimated by integrating over the frequency range from 100 Hz to 1 MHz; the rms phase noise of each signal output in the RF&CLK unit is listed in Table 2.

Table 2: Timing jitter and Phase noise integrated over from 100Hz to 1MHz of signals in RF&CLK unit.

Freq. [MHz]	Jitter (rms) [sec.]	Phase Noise (rms) [deg.]
1310	22.3 fs	1.0×10^{-2}
1300	16.0 fs	7.4×10^{-3}
40	573 fs	8.3×10^{-3}
10	1.14 ps	4.1×10^{-3}

Mixer & IQmod Unit

The mixer and I/Q modulator (Mixer&IQmod) unit includes two I/Q modulators (AD8349) for delivering the RF signal to the klystron, and ten active mixers (AD8343) for down-converting the RF signal from the cavity to the 10-MHz IF signal.

The temperature dependence of the components and the cable line in the analog units is an important factor to fulfil the condition of the accelerating electric field stability required during STF operation. A water-cooling system is adopted to stabilize the output signals of these RF&CLK and Mixer&IQmod units. The preliminary result about the relation between the water temperature and the fluctuation of output signal was about 0.1 deg./°C in the Mixer&IQmod unit. Because the water cooling system can regulate its water temperature within 0.1 °C, the signal will be stabilized within the order of 0.01 deg.

DSP & FPGA Board

The FPGA board installed on the DSP board is used for the real-time digital feedback control system. The DSP board, 'Barcelona' (Spectrum Signal Processing Inc.), is having four DSPs (TI-C6701) acts as a data/program exchange between the FPGA and the Host machine (CPU board). The data from the FPGA board are stored in

memories on DSP through the PEM (Processor Expansion Module) ports.

The FPGA board is made up of one FPGA chip (Xilinx, VirtexIIPro30), ten 16bit ADCs (LT2208) and two 14bit DACs (AD9764), as shown in Figure 4.

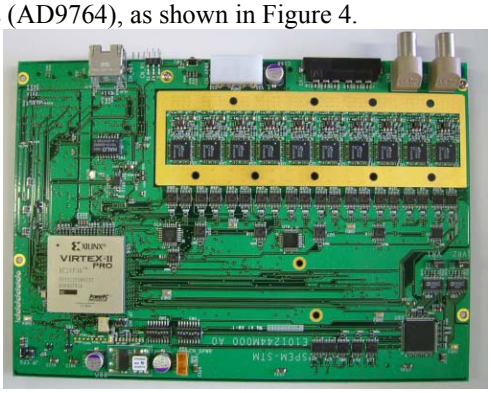

Figure 4: FPGA board.

In order to evaluate the FPGA board, a 10 MHz RF signal synchronized with a 40 MHz timing clock by a temporary RF&CLK unit was connected to the ADC in the FPGA board. Figure 5 shows the measured I/Q components of the 10-MHz RF signal. In this measurement, the top of the RF sine wave corresponds to the I-component. The errors of the I/Q components were ±0.07% and ±0.1%, respectively.

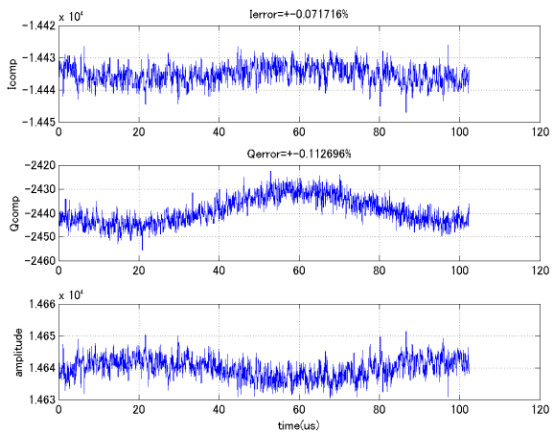

Figure 5: Measured I/Q components and amplitude of 10 MHz RF signal synchronized with 40 MHz clock of ADC.

A simple PI (proportional and integral) feedback control was adopted for the digital LLRF system. The software for the digital LLRF system is being developed and its development will be finished in the autumn of 2006. After completion of the software, a total performance test of the digital LLRF system will be carried out.

Cavity Simulator

In order to carry out a performance test of the digital LLRF system, a cavity simulator based on the FPGA board was developed, as already developed in DESY [5]. A commercial FPGA board (Nallatech, XtremeDSP Development Kit-IV) is used for this cavity simulator, which consists of one FPGA chip (Virtex-IV), two 14bit ADCs (AD6645) and two 14bit DACs (AD9772A).

In this cavity simulator, the cavity signal is estimated by calculating the state equation of the cavity in discrete form. Figure 6 shows the cavity output signal modulated with the IF frequency.

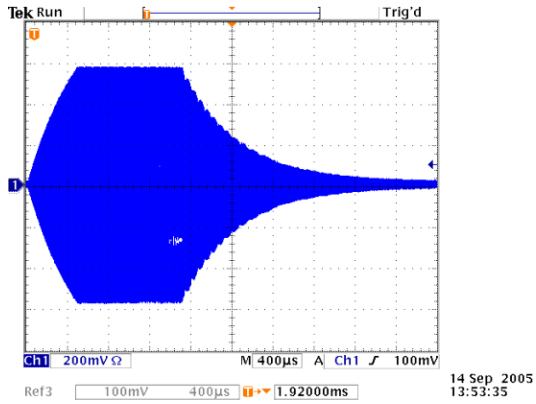

Figure 6: Cavity output signal modulated with IF frequency

SUMMARY

In STF Phase-I, the LLRF system, except for the digital RF control system, has been operated for high-power testing of the klystron and couplers installed in the superconducting cavities.

An accelerating electric field of 0.3% (rms) in amplitude and 0.3 degree (rms) in phase are also required in STF Phase-I. The digital LLRF control system using FPGA is adopted to satisfy these requirements. The components required for the digital LLRF system have been developed, and their performances have been evaluated. A total performance test of the digital LLRF system using a cavity simulator will be carried out in the autumn of 2006.

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