COMMISSIONING OF THE DIGITAL LLRF FOR THE CEBAF INJECTOR/SEPARATOR

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Abstract

The design and production of the 499 MHz digital Low-Level RF control system for the CEBAF accelerator has been completed. The first five systems have been installed for use with the CEBAF Separator RF deflecting cavities operating at 499 MHz. The next four systems were installed in the injector on the chopping cavities (also 499 MHz deflecting cavities). The new LLRF system replaced an analog system that was over 15 years old. For initial testing, an extensive acceptance plan along with a LLRF test stand was developed and incorporated to assure system performance as well as reliability. Various VHDL firmwares were developed to support operation of this system and included specific operational diagnostics. Once the acceptance tests were completed, the new systems were installed in the accelerator in parallel with the existing analog LLRF for extensive in-situ testing and comparison. Once commissioned, the new RF systems were assigned to the CEBAF accelerator and turned over to Accelerator Operations. This paper will address the VHDL firmware evolution, the automated tests, and the performance measurements made throughout the installation and commissioning process.

REQUIREMENTS AND DESIGN

RF Requirements

The chopper and separator cavities are both beam deflecting cavities. In the case of the chopping cavities, two orthogonal modes (Q_L=11,000) are excited in a single copper structure, with mode isolation being greater than 40 dB. The electron beam is chopped and then de-chopped after the beam has been modified. The separator cavities use a TEM dipole mode (Q_L=2500) that can deflect multiple beams. The field control requirement for these cavities is relatively undemanding at 1% and 1 ps RMS amplitude and phase control respectively. In the case of the chopping cavities the amplitude is rarely changed, but in the case of the separator, amplitude is adjusted to produce the deflection needed for different beam energies. See Table 1 for cavity characteristics.

Temperature induced phase drift of the receiver should be lower than 0.1° per 1°C

Table 1: Cavity Characteristics

	Chopper	Separator
f_0	499 MHz	499 MHz
r/Q	14.4 Ω	$44.7\,k\Omega/m \times 0.3m = 13410\,\Omega$
Q_L	10000	2500

Digital RF System Description

Figure 1 is a picture of the low level RF control system (LLRF). This architecture has become the common model for single cavity control LLRF systems, with 4 RF inputs and 2 RF outputs utilizing a modern large field programmable gate array (FPGA). We have chosen the VXI platform for both convenience and its RFI/EMI properties. The system utilizes a mother - daughter board with the FPGA on the motherboard and the daughterboard hosting the RF hardware, analog to digital and digital to analog converters for both the receiver and transmitter. The RF system down converts the cavity frequency of 499 MHz to an IF of 70 MHz. This allows us to use the local oscillator (LO) and IF signals that are already distributed around CEBAF. The receiver IF signals are then quadrature demodulated using harmonic undersampling (56 MHz clock). The transmitter output is a single IF output at 70 MHz where the quadrature components are digitally recombined inside the FPGA .

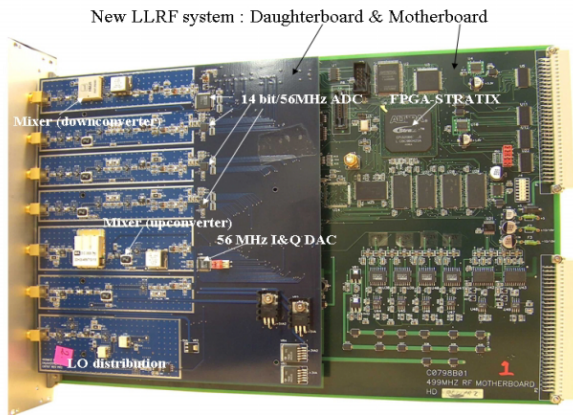

Figure 1: LLRF system.

ACCEPTANCE TEST PROCEDURE

Subsystems to be Tested

Motherboard/FPGA

The testing of the LLRF motherboard is fully automated. The FPGA is configured through a JTAG cable as a NIOS softcore processor to run a C program . Various loop-back tests are performed. Status updates are

displayed on a PC pinpointing failed component(s). The program takes ten minutes to run through all of the tests.

56 MHz PLL clock synthesis

The characterization of phase noise (timing jitter) of clocking sources is crucial due to their direct impact on the performance of the data conversion devices (A/D and D/A). Once the time jitter is measured (typically 500 fs) we can calculate signal to noise ratio (SNR) using the following formula:

$$SNR = -20 \times \log(2 \times \pi \times f \times t_{jitter}) = 75$$

One can also calculate the ideal SNR based on number of bits (12):

$$SNR_{ideal} = 6.02 \times N_{bits} + 1.76 = 74$$

At 500 fs, the clock jitter has not exceeded the required SNR specification of 60 dBc. Even for a clock t_{jitter}= 1 ps, the SNR = -67 dBc and is still below the required -60 dBc. The phase noise measurement was made using an Agilent E5052A Source Signal Analyzer. In all cases the integrated RMS time jitter measured for 10 Hz -1 MHz bandwidth stayed below 1ps.

RF Transmitter

The dynamic range, spectrum and linearity were checked as part of the test. We focused on the spurious inter-modulation which could indicate clock instability, crosstalk, LO leak etc. In all systems we measured spurious output below -60 dBc.

RF Receivers

Detailed measurements were necessary to characterize dynamic range, linearity, and crosstalk. A two tone IP3 test was completed to obtain figure-of-merit for linearity and distortion. In addition, the receivers were cycled through an environmental chamber to measure temperature-induced phase drifts. The receivers exhibited on average of 0.1º of phase shift per 1ºC.

VHDL Firmware and EPICS

Initially, a number of VHDL programs were created to troubleshoot hardware followed by basic control algorithm. Weeks of intense testing led to multiple firmware modifications which ultimately produced a robust firmware design. Numerous tests were performed to verify functionality of the EPICS software. These tests included open loop test, closed loop test, loop gain/bandwidth characterization, and phase coherence after a system crash or power down.

Test Stand and Procedure

Fig.2 shows a typical diagram of the LLRF Test Stand. This setup could vary depending on the specific measurements requirements.

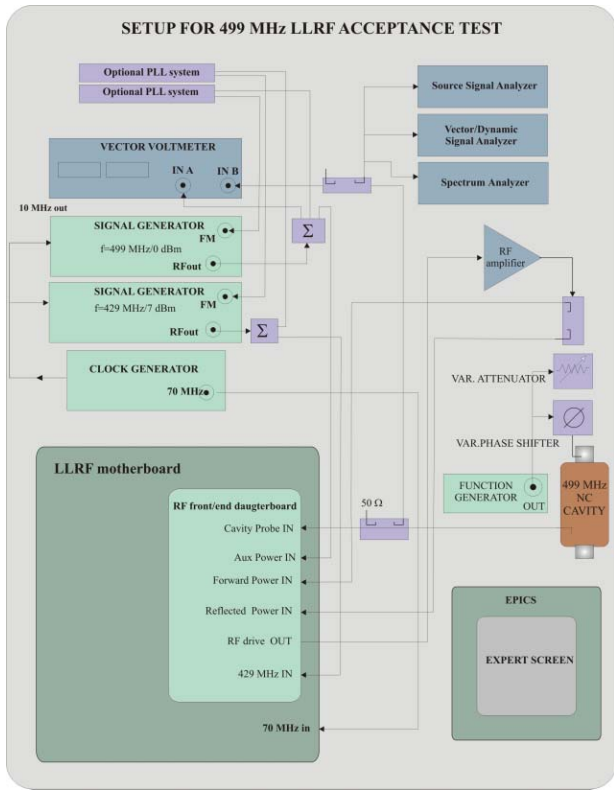

Figure 2: Acceptance test setup.

In general, the LLRF module and IOC card are installed in the deep-VME chassis. 20 dBm /429 MHz LO is provided from a generator as well as a 70 MHz reference for clock. All instrumentation is located in one rack. There are two types of communication used for testing: Ethernet for EPICS software, and JTAG with Altera/Quartus software for basic hardware troubleshooting. Next to the rack we placed a 499 MHz normal conducting cavity, high power amplifier, phase shifter and variable attenuator. The phase noise measurement was made using an Agilent Source Signal analyzer. Dynamic range and linearity measurements were characterized with an HP Vector Voltmeter. Spurious measurements were made with a Spectrum Analyzer or Source Signal Analyzer. The loop bandwidth was determined using a Dynamic Signal Analyzer. Figure 3 shows the loop bandwidth of the system. During acceptance test all data, measurements and notes were collected in the specific document for further analyzing and assessment. Any problem required a subsystem to be sent back for repair then the test was repeated. Once that subsystem was functional, the LLRF system was again sent through the complete acceptance procedure.

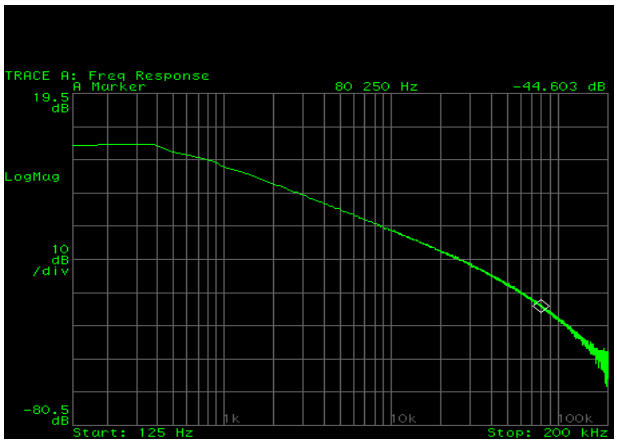

Figure 3: System loop bandwidth.

COMMISSIONING AND OPERATION

Installation

New modules were installed in the deep VME chassis and all RF connections were transferred to them. New EPICS software was uploaded and all necessary parameters and data were typed into the Expert Screen. Due to limited accelerator down time and the necessity of having a simple back-out procedure, the old analog LLRF system remained in place.

Commissioning

Measurements and optimization

The RF system was commissioned starting with the feedback loop and the digital clamp set at a low (safe) power level. Forward and reflected RF signals were continuously monitored during this stage. We set all the regulation parameters based on the acceptance test experience.

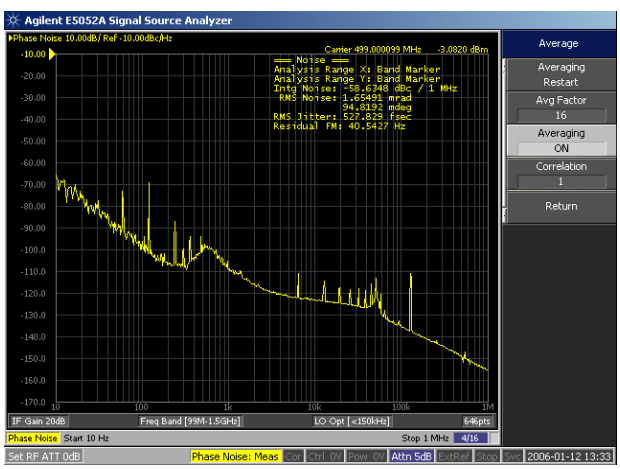

Figure 4: Phase noise.

Once the system was stable in open loop mode the feedback loop was closed. With the loop closed we optimized proportional and integral gain by minimizing amplitude and phase noises. The optimized power spectral density of phase noise signal and its integrated RMS value measured for the chopper cavity is shown in Fig. 4. During testing we found a noticeable noise contribution from the 70 MHz reference used to synthesize the 56 MHz sampling clock. A modification to the MO distribution path eliminated this problem. Phase noise values between 500 and 800 fs were measured for all the modules, easily meeting our specifications. Spurious signals at 60 and 120 Hz were also observed but were far enough down not to cause any problems. Noise from the VME power supply caused additional 56 MHz clock jitter noticeable just above 100 kHz. Modifications to the board capacitors minimized this effect. We believe some spurious signals between 10 kHz-100 kHz are caused by quantization effect inside the FPGA (limit cycling due to round-off in multiplication causing dead-band effect). Additional improvement was also limited by phase noise from the 427 MHz LO signal as well as from the 70 MHz clock reference.

Operation

All systems were brought into operation using an EPICS operator screen. Functionality of the automated RF ON procedure, “operator sliders” for amplitude and phase setup, as well as interlocks were verified. Performance of the automated rotation matrix was checked with insertion of +/-90 and greater degrees phase shift into the probe line, during which the system is expected to remain stable. Finally, the digital LLRF systems were turned over to Accelerator Operations for regular use.

SUMMARY

The digital LLRF systems were successfully built, tested and put into operation in the CEBAF accelerator. They were entirely designed by the EES RF group in order to best match the operational constraints and specific requirements of these sections of the Accelerator. Completion of such a project was beneficial in expanding the knowledge and expertise of our RF group. The technology and experience gained will be used in the design of the superconducting LLRF version as a part of our 12 GeV energy upgrade project.

REFERENCES

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