MASTER OSCILLATOR FOR FERMILAB ILC TEST ACCELERATOR

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Abstract

The low phase-noise master oscillator (MO) generates and distributes the various frequencies required for the LLRF system controlling ILC Test Accelerator (ILCTA) cavities. Two chassis have been developed for this design, generating the programmable frequencies and performing the distribution and amplification, respectively. It has been successfully used with the SNS and the DESY-SIMCON LLRF systems, driving two different superconducting cavities. The design approach and characterization of the master oscillator are presented in this paper. The measurement results include the phase and amplitude noise spectrums of the multiple frequency outputs.

INTRODUCTION

Due to the early stage R&D for the ILC, the chosen approach in designing the master is to give priority to versatility and flexibility. All necessary frequencies and their use will not be known until the design is final. For this reason we opted for a design based on a programmable clock distribution. This document will present in the first part the overall description of the master oscillator, while the second part will focus on the phase noise measurements.

DESCRIPTION OF THE MO

In order to accommodate for several projects currently underway at Fermilab, the MO provides nine frequencies listed in Table 1. The required frequencies are indicated, as well as the number of corresponding outputs and desired power levels. The MO consists of two chassis dedicated to generating the clock frequencies and distributing and amplifying the different signals. We chose to isolate the power supply in a separate chassis to provide additional magnetic isolation from the 60 Hz line and harmonics.

Table 1: frequency requirements for the MO

Freq. MHz	Power dBm	Out Nb.	Description
1300	+13	3	Cavity RF reference
325	+13	3	Proton driver Cavity Reference
86.7	+13	3	ADC Clock
81.3	+13	3	Source Laser
50.0	+13	3	IF
9.03	TTL	2	Clock System Source
3.09	TTL	2	Beam bunch rate
1.00	TTL	2	Clock System
0.25	TTL	2	SIMCON IF

Clock Frequencies Generation

Rather than multiplying up from a stable reference oscillator, a divide down approach was chosen for this project. The motivation behind this choice was to reduce the wide band phase noise that is present in a multiply up scheme. The schematic layout of the MO clock distribution chassis is given in Fig.1. The design is based on the clock distribution chip AD9510 [1]. This low phase noise chip has eight configurable outputs with programmable frequency dividers, adjustable delays and an integrated phase lock loop (PLL) core. The outputs (LVDS/CMOS) have a programmable divider that can be bypassed or set to an integer up to 32 and deliver sub-harmonics of the input frequency. In order to provide all nine required frequencies, three evaluation boards of the AD9510 have been daisy-chained as indicated in Fig.1. Synchronization between the boards and their outputs is ensured using an external triggering sequence. A 10 MHz crystal oscillator from Wenzel Associates [2] is being used as a phase reference and a 1300 MHz dielectric resonator oscillator (DRO) from Poseidon Scientific Instruments [3] is locked on the crystal reference via the PLL. The purpose of this set up is to benefit from the frequency stability and close-end low phase noise of the crystal combined with the wide-band low phase noise of the DRO.

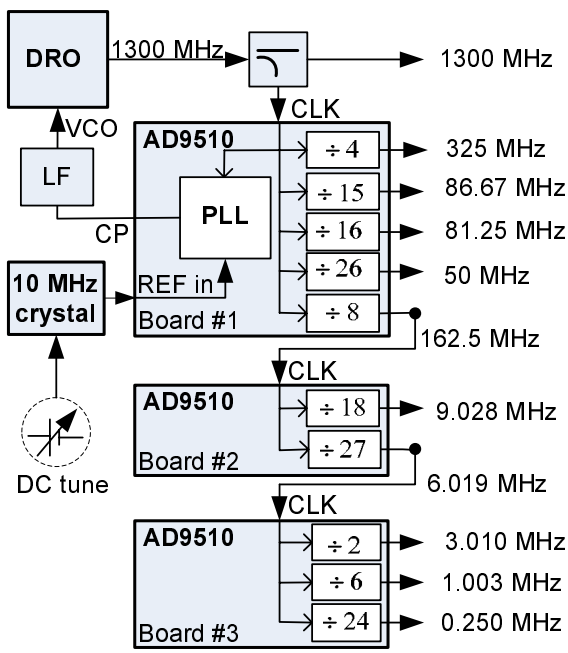

Figure 1: Schematic layout of the clock generation.

The DRO has an integrated voltage controlled oscillator (VCO). The control voltage delivered by the charge pump (CP) output of the PLL is filtered and amplified by a loop filter (LF) circuit before being directed to the VCO. This LF is a third order active design with low noise components in order to minimize its additional phase noise contribution. It was done according to the design and simulation tool, ADIsimCLK, provided by Analog Devices [4]. The 10 MHz crystal also has a built-in VCO designed to adjust the RF frequency to the cavity resonance frequency. At 1300 MHz, the electrical tuning range was measured to be ± 390 Hz, combined with a mechanical tuning range of ± 1.82 kHz. This VCO input is used as the control point for the phase noise measurements.

Signal Distribution and Amplification

In order to supply enough outputs at the required levels, an additional chassis was developed to split and amplify the different signals. For the non-TTL outputs, an individual IC board was developed for each frequency signal and placed into individual shielded housing to minimize possible cross talks. Each signal is first split in four (three outputs and one monitor) then amplified to be brought up to +13 dBm. For the TTL outputs, a separate board was designed to change the differential signals to single-ended output.

RESULTS

The first step consisted of measuring the phase noise spectrum of a single chassis. This was done using the phase-noise mode of the Agilent Technologies PSA spectrum analyzer [5]. Figure 2 shows the phase noise measured at 1300 MHz before and after the power supply is being placed in a separate chassis.

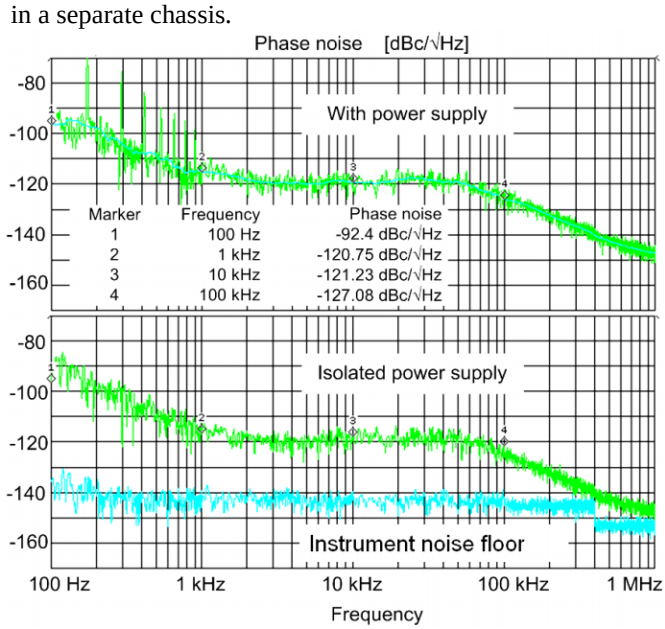

Figure 2: 1300 MHz phase noise.

As can be seen, the 60 Hz and its harmonics have been removed. The phase noise values for the 1.3 GHz signal are found to be -92 dBc/√Hz, -120 dBc/√Hz, -121 dBc/√Hz and -127 dBc/√Hz at 100Hz, 1kHz, 10 kHz and 1MHz respectively. At this point the measurement is just showing the noise floor of the spectrum analyzer.

To measure the absolute phase noise performance of the system, two identical MO have been built. Corresponding frequencies are then connected to a noise analyzer, the Wenzel Associate BLUEPHASE 1000™. One MO is treated as a reference while the other is the device under test (DUT). The noise analyzer has an integrated PLL that locks onto the reference MO, while controlling its frequency by means of the 10 MHz crystal VCO. This signal is then mixed down with the corresponding frequency from the DUT. The phase noise is down converted to base band and amplified (+60 dB) to raise the signal level above the spectrum analyzer floor noise level. The setup of this measurement is depicted in Fig.3.

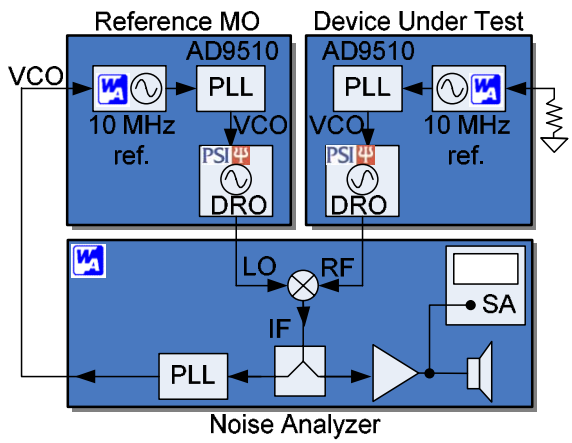

Figure 3: Absolute phase noise measurements setup.

Figure 4 shows the phase noise measurement obtained with and without the AD9510 control PLL. In the case without the PLL, one DRO is free running, while the second is being controlled by the noise analyzer. In the second measurement, the DRO of both master oscillators are now individually locked onto their 10 MHz reference via the AD9510 PLL. In either case, the RF distribution and amplification chassis is included in the loop, so as to measure the phase noise of the total system, including any phase noise contribution associated with amplifying and splitting the signals. While doing the measurements, we noticed that the DROs tend to "talk" to each other if the MOs are insufficiently isolated. In this particular situation, the DROs lock onto each other, artificially improving the overall phase noise performance of the system. The amplifiers and splitters from the RF amplification and distribution chassis provide enough isolation to prevent cross talk between the DROs.

Fig. 4 shows the measured noise performance of the 10 MHz crystal oscillator. The noise values are normalized to to 1300 MHz. The measured noise performance of the DRO is also shown. As can be seen, the benefits of the PLL are significant below 100 Hz. However, the loop filter also adds noise in the 100 Hz - 10 kHz range, degrading the system overall noise performance. Above 10 kHz, the noise discrepancies between the designs with and without the LF become negligible. As an indicator, the expected noise level from the ADIsimCLK simulation is also shown in this plot. Further investigation is required to fully understand the sources of noise in this design. Future work includes narrowing the bandwidth of the loop filter and increasing the loop gain to reduce the sub-kHz noise level.

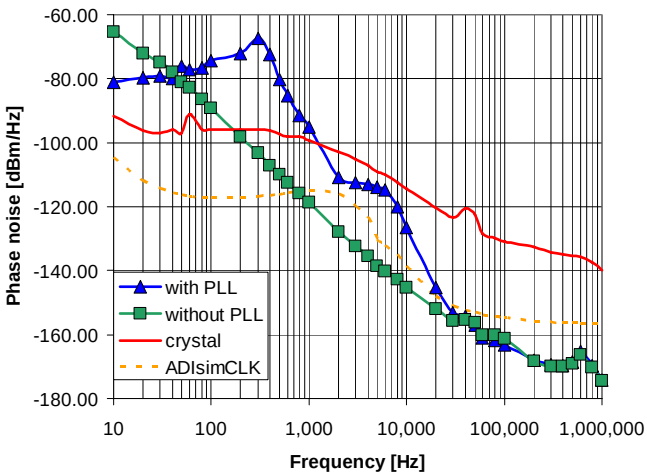

Figure 4: Absolute phase noise of the MO with and without the crystal reference.

CONCLUSION

We have developed a programmable low phase noise master oscillator for the ILC Test Accelerator. A functional description of the master oscillator and its architecture was given. Absolute phase noise measurements were performed and the measurement techniques explained. Although some improvement has been made towards higher phase noise performance, the presented design does not currently meet the requirements specified for the international linear collider. However, the authors believe that the current design is viable and that further investigation on the sources of phase noise within this architecture should permit to meet these requirements in a timely manner.

ACKNOWLEDGEMENTS

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REFERENCES

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[2] Wenzel Associates crystal oscillator http://www.wenzel.com/datasheets/uln/501-04538.htm
[3] Poseidon Instruments DRO http://www.psi.com.au/Pages/ProductPages/OscillatorProducts/DROOscillator.html
[4] ADIsimCLK http://www.analog.com/en/content/0%2C2886%2C1073%255F931%255F67762%2C00.html
[5] Agilent Technology PSA spectrum analyzer http://www.home.agilent.com/USeng/nav/-536902959.536881890/pd.html