# A COMPUTER-STORAGE SCOPE DISPLAY INTERFACE

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## ABSTRACT

This discussion describes a computer interface for a graphical storage-tube display. The technique allows X-Y point display with intensity control as well as X-Y point plotter hard copy.

Conventional computer software generates binary data for the interface hardware. The interface controls the storage scope plotting through internal timing and sequencing circuits. X and Y point positioning for the scope and optional plotter are accomplished with interface digital-to-analog converters.

## Introduction

Storage tube graphical displays provide a valuable means for communicating information to the NAL linac operator through the control computer. This paper describes the display interface used between the XDS Sigma 2 computer and the Tektronix 611 storage scope. Interfacing to the Hewlett-Packard type 7004A X-Y point plotter is provided by the same system. With the addition of the Tektronix 4501 scan converter, TV graphic displays are available. The Tektronix 4601 hard copy unit provides rapid graphical displays on paper.

The design of the display interface is matched to the Sigma 2 computer so that only a minimum of instructions is required to plot a point on the display. The actual plotting of the point is overlapped with instruction execution for maximum speed. Character generation and line drawing is handled by the software. Characters based on a 5 x 7 dot matrix can be displayed in less than 1 msec. Lines may be drawn at about 25 $\mu$sec per point.

The computer talks to the display interface through five digital stored output modules (DSOM's). Each DSOM is simply an 8-bit register with drivers. Four DSOM's are required for setting the X and Y hybrid digital-to-analog converters (DAC's). The other DSOM is used to select the various functions of the display interface, such as display erasing and plotted point intensity.

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The interface uses all TTL integrated circuits. The intensity control is accomplished by using monostable multivibrators and retriggerable monostable multivibrators (monos) to vary the length of the store pulse. This technique eliminates internal software computer timing.

## Operation

Figure 1 is the circuit and logic diagram for the interface. The point-store timing and sequencing is accomplished by M14, M15, and M16. The three monos interact to provide correct timing to prevent point-store overlap. The circuit also is adjusted with M16 to provide a minimum 6-$\mu$sec time interval between point stores. M14 automatically selects the time interval between M14 set at 24 $\mu$sec and M16 set at 6 $\mu$sec. M14 is connected as a retriggerable mono with a 100-$\mu$sec time interval window. Before a point-store is first initiated, the Q output of M14 is low. This low enables the first X or Y strobe pulse to operate M15. M15 generates a 24-$\mu$sec $\bar{Q}$ pulse output. The M15 $\bar{Q}$ output is the initial delay time before a point is stored on the storage scope CRT. The 24 $\mu$sec allows the X and Y DAC's to settle out and compensates for the time lag of the storage scope electron gun movement. If the second point position coordinate information and corresponding strobe occur within 100 $\mu$sec (the M14 time window), M14's $\bar{Q}$ output which has been forced high by the first pulse will inhibit M15 and prevent another 24-$\mu$sec delay while enabling M16 and initiating only a 6-$\mu$sec delay, which is adequate for plotting points close to the last one. When strobe pulses continue within the M14 time window, there will only be short delays between point stores, and a line or curve of closely spaced points can be drawn very quickly. When computer calculation time exceeds the M14 100-$\mu$sec time window, the M14 Q output goes low and permits M15 allowing another settle-delay time. The settle-delay time is always initiated at the beginning of a new presentation.

The "Nand" gate, A6, has $\bar{Q}$ inputs from M15 and M16. It therefore functions as an "Or" gate and permits either of the two delay pulses to energize the addressable intensity modulator. D1 is a one-of-four output decoder. The two-bit address (bits 6 and 7) from the computer selects one of four mono pulse width outputs. The storage scope CRT is intensity-modulated by store point pulse width. A short pulse width, 1 $\mu$sec, will not store on the CRT. A 5-$\mu$sec pulse width will store but will be very faint. A 25-$\mu$sec pulse width will store and will be bright. The "Nand" gate, C1, is also "Or" gate functioning and provides one of the four different pulse width outputs to the "store Z" input of the storage scope.

The interface prevents computer data overrun with three ready-level outputs to the computer DSOM's. Gate C2 is another functioning "Or" gate which has four information inputs:

1) Settle-time pulse width is a low input.
2) Store-Z point pulse width is a low input.
3) Erase-time interval from the storage scope is a low input.
4) Point plotter plot time is a low input.

Whenever any one of these inputs is low, the interface is busy, and the computer SDOM is informed of the busy as a low level. When the level goes high, the computer can renew the data on the X or Y DAC inputs and generate new strobes to accompany the data for the next graphical display, point store, or point plot.

The storage scope CRT is rectangular. The X-Y DAC outputs produce a square format. In order to make maximum use of the rectangular CRT, bipolar DAC's are used. This allows the program to send negative X or Y voltages to plot outside the normal display area. This design maximizes the available information area.

When the "plotter enable" switch is operated, the A7-A8 R-S flip-flop starts the X-Y point plotter. The null detector has a special modification to insure proper operation. The "ready" output is an extra pole on the "on-off" switch. When the "on-off" switch is in the on position, the null detector $V_{CC}$ is applied to the B1 gate and F1 flip-flop "clear" input. If the "on-off" switch is not in the proper position, plot enable is prevented, and an erroneous busy at the input of C2 is avoided. The F1 Q output enables the null detector at the "enable/disable" input, permits A9 to pass the X or Y strobe pulses to the "+ seek" input of the null detector. The strobe pulses also set the A11-B2 R-S flip-flop for the busy indication at C2. When the point is plotted on the paper and the pen lifted for the next point (the M12-M13 delay time allows complete pen lift for proper operation), a "complete" output pulse is generated by the null detector. The "complete" pulse resets the A11-B2 R-S flip-flop and C2 is issued a ready level so the next point may be plotted.

Operation of the point plotter may be stopped by re-pressing the "plotter enable" switch or by having the computer generate an "end plot pulse." M11 produces the stop reset pulse to the A11-B2 R-S flip-flop.

Buttons on the system include the visual on/off function and three operation switches.

1) The "erase disable" prevents the computer-generated erase function from erasing the CRT and allows display overlays.
2) The "busy disable" is the bail-out function. It is a temporary ready switch in case of computer or interface hang-ups. It is generally operated as a trouble diagnostic aid.
3) The "plotter enable" permits X-Y point plotter hard copy operation.

## Computer Outputs and Inputs

Bit 0, the "settle delay always," defeats the automatic sequencing circuit of M14, M15, and M16. The time interval between point stores is fixed by M15 at 24 μsec, the settle delay, which means a slow overall presentation.

Bit 1, the "write thru," allows plotting points which do not store on a stored display. One application of this would be a non-storing cursor used as a pointer to allow the operator to communicate with the graphical display.

Bit 2, the "non store," allows use of the display as a large screen oscilloscope. The points obtained are very bright. The obvious disadvantage is that the display is not stored but must be constantly refreshed.

Bit 3, the "strobe address," permits selection of the X SDOM strobe pulse instead of the Y SDOM strobe pulse. When plotting an X-axis line, this means that only the X-DAC's need be set by the computer as the points are plotted. Without this feature, dummy Y outputs would be required for each point to provide the strobe pulse which results in the point being plotted.

Bit 4, the "erase," initiates the erase of a display prior to generating a new display.

Bit 5, the "end plot pulse," resets the X-Y plotter at the end of a display.

Bits 6 and 7, the "intensity address 0" and "intensity address 1," allow the computer to select one of four different point store intensities. This feature is used to distinguish between prime data and display backgrounds.

The X and Y pulses are point-store strobes. The leading edge of the pulse occurs at approximately the time of SDOM data output flip-flop change. The trailing edge of the pulse indicates that the data is stable.

The "plotter enable binary sense" informs the computer that a plot is being presented and insures that bit 5, the "end plot" pulse, is properly generated.

The "busy/ready level" is an input to the SDOM which, when busy (low), inhibits any input data change from affecting the SDOM output.

## Hardware

Inputs are from the XDS Sigma 2 type 7950 eight-bit stored output modules (SDOM). The system requires:

a) two SDOM's for the X-axis store.

b) two SDOM's for the Y-axis store.

c) one SDOM for the control word.

Interface outputs operate into the following display devices:

a) one Tektronix type 611 storage display unit.

b) one H-P type 7004A point plotter with dc input modules 17170A and and 17170B, null detector 17173A, and point plotter 17012A.

c) one Tektronix type 4501 scan converter unit for operating B & W TV monitors.

d) one Tektronix type 4601 hard copy unit for fast actual size hard copy presentations.

The "knob" (see Fig. 2) is the principal means of analog control in the linac control room. The knob is a digital shaft encoder. The function of the "knob" is discussed by R. W. Goodwin in his paper.[1] The operation is described by E. Anderson et al., in their paper.[2]

The boxes used to house the interface, "knob," and function buttons are standard NIM modules.

Eleven visible light-emitting diodes and five test points are mounted on the interface front panel as operational indicators.

The interface uses TI 7400 logic[3] and FCS[4] type 9601 and 9602 monos. The one-of-four decoder is an FCS 9321.

Various resistors and zener diodes are used in the interface circuit to match currents and voltages to the outside devices.

The cost of the interface circuit excluding the output devices is approximately $500.

## ACKNOWLEDGMENTS

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## REFERENCES

[1] Robert W. Goodwin, NAL Linac Control System Software, Proc. of the 1970 Proton Linear Accelerator Conference, National Accelerator Laboratory, p. 371.

[2] Elton W. Anderson, Hong C. Lau, and Frank L. Mehring, The Computer Monitoring and Control System for the NAL 200-MeV Linac, Proc. of the 1970 Proton Linear Accelerator Conference, National Accelerator Laboratory, p. 451.

[3] TI, Texas Instruments, Inc.

[4] FCS, Fairchild Semiconductor.

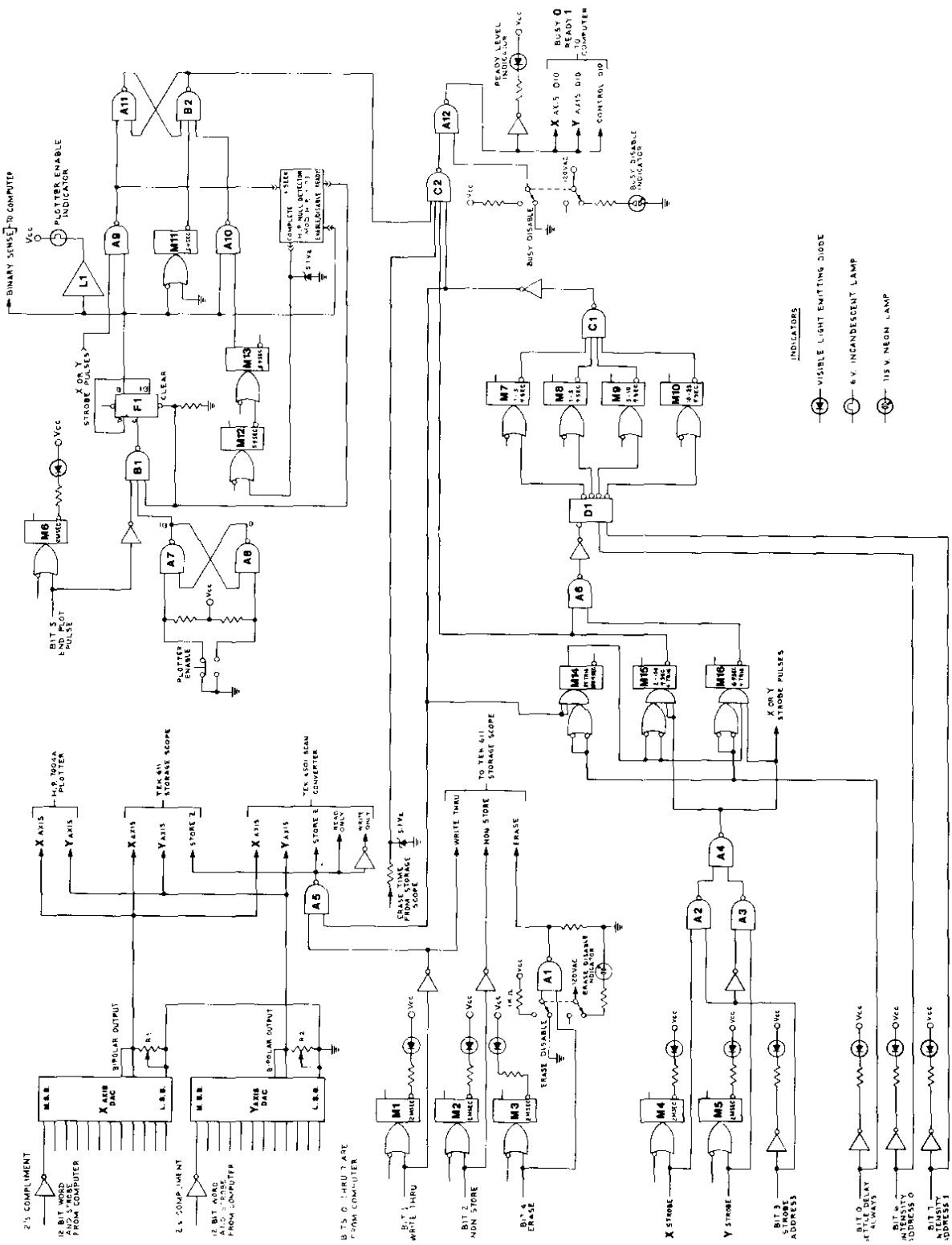


Fig. 1. Combined logic and circuit diagram of the computer-storage scope display interface.

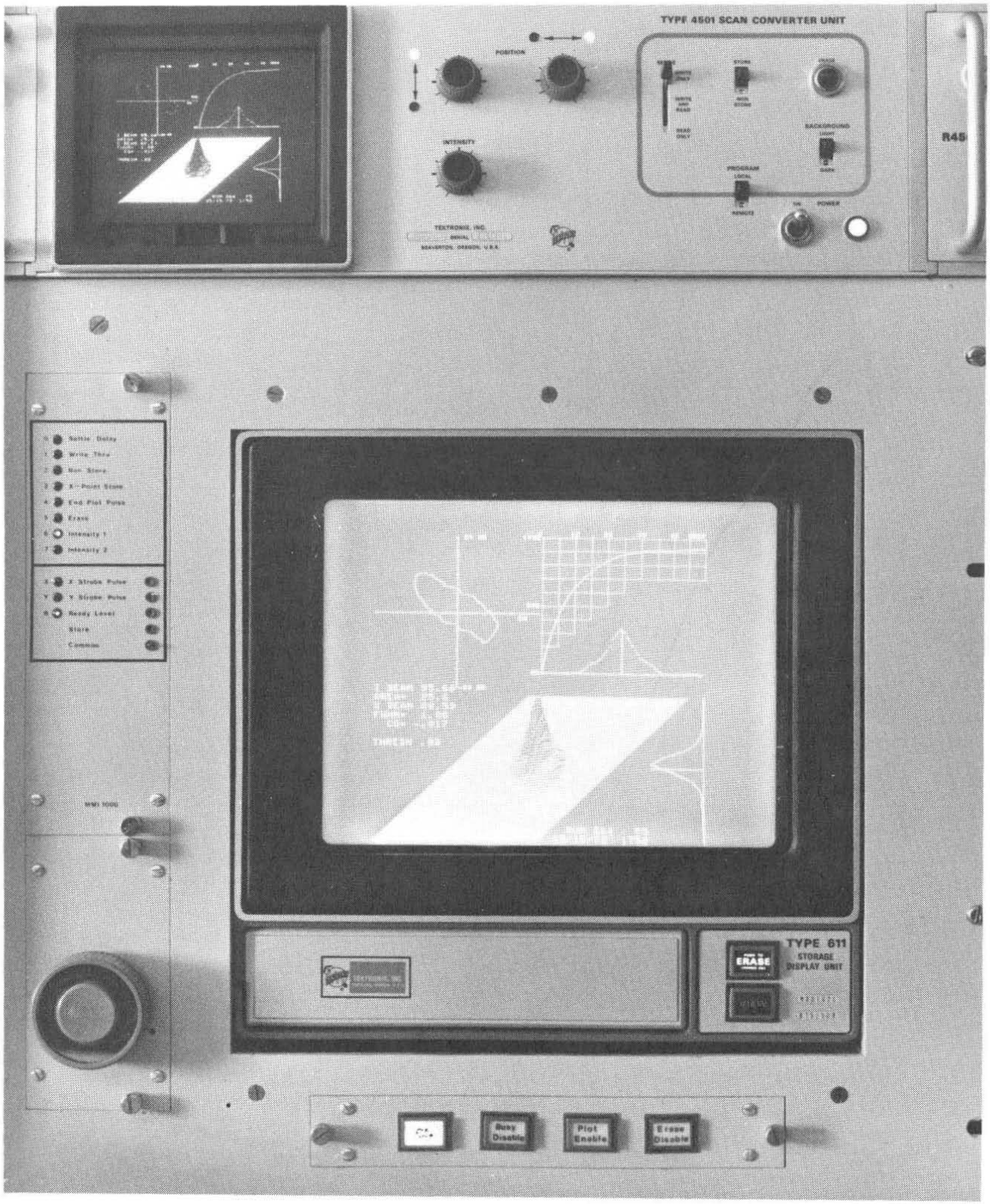


Fig. 2. The interface with storage scope and scan converter displaying an emittance plot.