DEVELOPMENTS OF THE RF SYSTEM FOR THE FUSION MATERIALS IRRADIATION TEST ACCELERATOR*

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Summary

The rf system for the Fusion Materials Irradiation Test (FMIT) accelerator is currently in the design phase at the Los Alamos Scientific Laboratory (LASL). The 35-MeV, 100-mA deuteron beam will require approximately 6 MW of rf power at 80 MHz. The EIMAC 8973 power tetrode, capable of a 600-kW cw output, has been chosen as the final amplifier tube for each of 15 amplifier chains. The final power stage of each chain is designed to perform as a linear Class B amplifier. Each low-power rf system (≤100W) is to be phase, amplitude, and frequency controlled to provide a drive signal for each high-power amplifier. Beam dynamics for particle acceleration and for minimal beam spill require each rf amplifier output to be phase controlled to ±1°. The amplitude of the accelerating field must be held to ±1%. A varactor-tuned electronic phase shifter and a linear phase detector are under development for use in this system. To complement hardware development, analog computer simulations are being performed to optimize the closed-loop control characteristics of the system.

General Description

Preliminary rf system design for the linear accelerator (linac) portion of the FMIT facility is in progress.[1] The 35-MeV accelerating structure will consist of a low-beta radio-frequency quadrupole (RFQ) accelerator and buncher[2] up to 2 MeV followed by two post-coupled Alvarez tanks in series, with an intertank spacer at the 20-MeV point. The 35-MeV, 100-mA cw deuteron beam will require approximately 6.0 MW of rf power at 80 MHz.

The basic layout of the FMIT rf system includes a total of 15 power amplifiers driving three linac tanks.[3] Each rf amplifier chain will be capable of generating at least 600 kW of power. The RFQ will require two amplifier chains and each linac tank will need at least six or seven. A multiplicity of drive loops will be used for inductively coupling the rf energy into the accelerator tanks. Each power amplifier (PA) will have its own coupling loop.

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Phase Control System

The output of each rf amplifier must be controlled to ±1° in phase. A diagram of the amplitude and phase control system is shown in Fig. 1. The major components of this system are a 400° electronic phase shifter, a linear rf phase detector, and a phase controller.

Electronic phase shifter

A schematic of the phase shifter is shown in Fig. 2. The phase shifter is a varactor-tuned, circulator-type device, similar in principle to those used at the Clinton P. Anderson Meson Physics Facility (LAMPF). Because of the non-existence of ferrite components (circulators) at 80 MHz, it was decided to build the phase shifter to operate at 400 MHz. This makes it possible to utilize strip-line techniques. A double-balanced mixer on the input is used to heterodyne the 80-MHz signal with a 320-MHz signal to produce the 400 MHz required by the phase shifter. The 320 MHz is derived by frequency quadrupling a portion of the 80-MHz input.

The 400-MHz signal enters Port 1 of the 4-port circulator. Ports 2 and 3 are terminated with varactors and the appropriate lengths of transmission line. Port 4 provides the 400-MHz, phase-shifted output. This signal then is heterodyned back to 80 MHz. All phase information is preserved because the same 320-MHz signal is used for both up and down conversion. An experimental model of this phase shifter has been operated successfully with 400-MHz inputs from 0.1 to 1.0 watt.[4] This phase shifter exhibits a linear response with a 400° range, as the dc bias is varied from 0-40 volts. The insertion loss varies from 2 to 5 dB. Figure 3 illustrates the measured phase shift and insertion loss versus varactor bias.

Linear phase detector

A linear phase detector is under development for use in the feedback control loop. The output will be a dc level between ±10 volts, linearly proportional to the phase difference between the two inputs. The detector must have 0.5° resolution, a 360° range, and a 100-kHz bandwidth.

Basically, the phase detector generates, then integrates the waveforms shown in Fig. 4. These are variable duty-cycle square waves whose signs are determined by whether the signal is leading or lagging the reference. The waveform is then integrated to produce a dc level

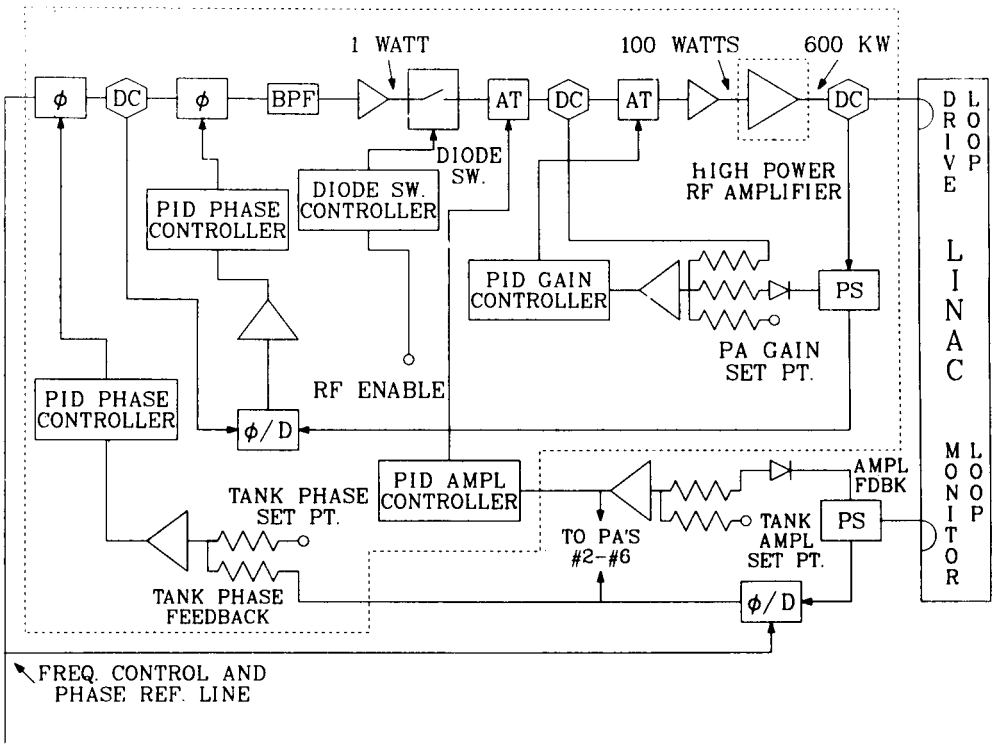

Fig. 1. A single rf amplifier chain.

proportional to the duty-cycle. For example, when the signal (SIG) and reference (REF) are in phase, a symmetrical square wave is produced that integrates to zero. When SIG leads REF, the square wave becomes asymmetrical with an increasing positive pulse width proportional to the phase difference between the two inputs. This will integrate to a positive dc level.

Figure 5 is a simplified schematic of the phase detector. Both the 80-MHz REF and SIG are mixed with a 79-MHz local oscillator signal to produce two 1-MHz signals that retain the same phase information as the 80-MHz inputs. Each 1-MHz signal passes through a voltage comparator to generate a 1-MHz square wave. A D-flipflop is used to provide a logic level that specifies whether SIG is leading or lagging. The SIG line goes to the D input of the flipflop and the REF line goes to the clock input. The flipflop changes output on the leading edge of the clock pulse, so, if the SIG is leading, the flipflop will output a high logic level and if lagging, a low. This bit addresses the multiplexer.

The waveforms of Fig. 4 can be realized by using SIG OR REF logic when SIG is leading and by using SIG AND REF when SIG is lagging. Only two multiplexer inputs need to be selected: x_0, which has the AND input, and x_1, which has the OR input.

The variable duty-cycle square-wave output of the multiplexer is then integrated, to produce a dc level proportional to the phase difference of the inputs. An alternate approach is being pursued in the event it is not possible to meet the ripple (<10 mV P-P) and bandwidth (100 kHz) specifications with an op amp integrator. This scheme would involve counting the time duration of the multiplexer output and using D-to-A conversion to generate a dc level from the counter output.

Phase control loops

Referring to Fig. 1, the phase control loop behaves in the following manner. The innermost phase control loop has a 50-kHz bandwidth and maintains a constant phase across the amplifier chain regardless of amplifier output power or other system fluctuations.

The outer phase loop is used to maintain the rf input to the accelerator at the proper phase for particle acceleration. A phase detector (ϕ/D) is used to compare the phase from an rf monitor loop in the tank, with the phase of a phase reference line. This dc output of the phase detector is sent to each PA driving that particular tank. This output signal is subtracted from a Facility Control System (FCS) computer-generated set point to produce an error

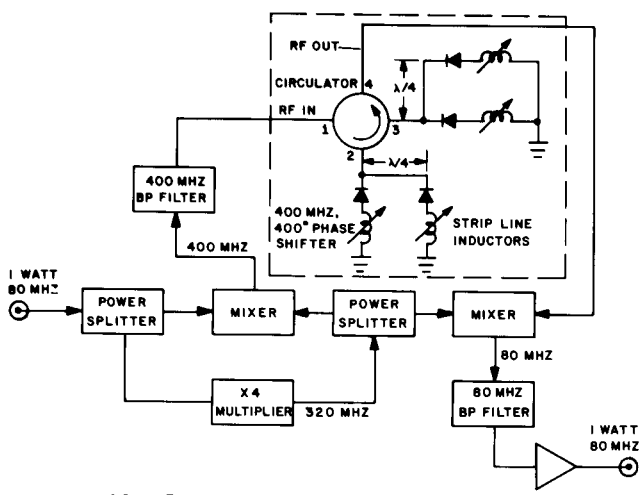

Fig. 2. An 80-MHz, 400° varactor phase shifter.

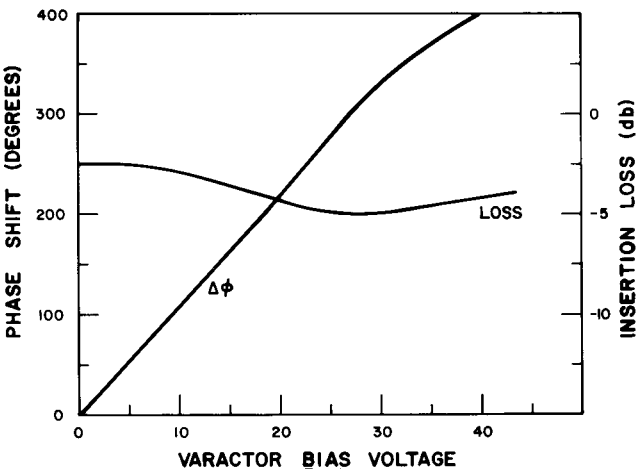

Fig. 3. Measured phase shifter characteristics.

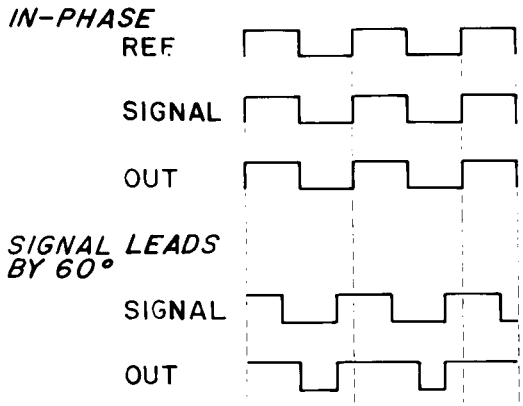

Fig. 4. Desired phase detector outputs before integration.

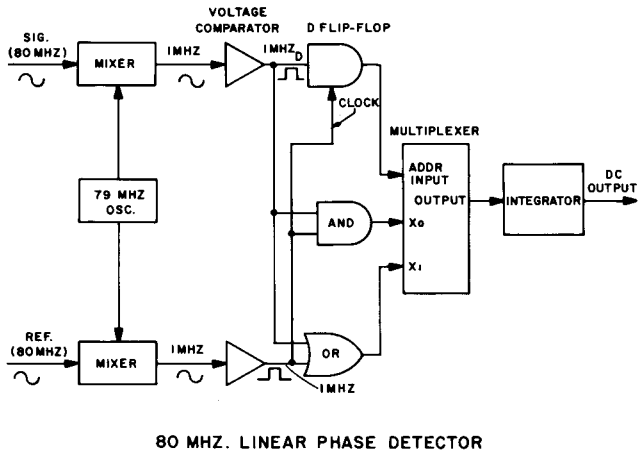

Fig. 5. An 80-MHz linear phase detector.

signal. Proportional, integral, and derivative (PID) compensation is used in a controller to transform the error signal into the proper voltage to drive the varactors in the phase shifters (ϕ), thereby forcing the error signal to zero. Analog computer simulation of the phase and amplitude control system is being done to determine the proper amount of compensation required for fast, stable, feedback loops. The bandwidth of this outer loop is about 10 kHz and it is determined primarily by the linac tank characteristics.

Amplitude Control System

The amplitude control system must maintain the accelerating field in each linac tank to within a $\pm 1\%$ tolerance. Two levels of control are required to do this. First, the overall gain of each rf chain must be maintained at a constant value regardless of the operating conditions (e.g., power output) of that chain. This is accomplished with an automatic gain-control feedback loop around each PA. Secondly, the power output of each PA must be adjusted to produce the required tank fields. Because each PA is a linear Class B amplifier, the output is strictly a function of the input drive level. An amplitude control system that monitors the field in the tank will control the output level of each PA.

Referring to Fig. 1, the amplifier preceding the diode switch is a leveling amplifier that provides one watt at 80 MHz under all operating conditions. This amplifier is necessary because the insertion loss of each phase shifter is not constant. With this arrangement, the rf signal into the diode switch has a constant amplitude and a variable phase. The diode switch is "open" except when the rf enable signal is applied. The output from the diode switch is passed through the voltage variable attenuators (AT), which are the control elements for the

amplitude and gain control circuits; the output signal from the last attenuator drives the constant-gain solid-state amplifier. The output from this amplifier (1 to 100 watts) drives the high-power rf system.

Because FMIT has up to seven amplifier chains per linac tank, each amplifier chain must have the same gain. This gain also should be independent of output power level. To accomplish this for each PA, the forward power from the PA is measured and is compared with a power sample taken from a directional coupler (DC) between the two attenuators. The ratio of the former to the latter is the gain of the system between those two points. This value for the actual gain is compared with an FCS computer-generated gain set point. If the actual gain is not equal to the desired gain, an error signal is produced that is acted upon by the PID gain controller. The controller adjusts the attenuator nearest the PA to drive the error signal to zero, thereby producing the desired overall gain through the power amplifier system. This automatic gain control system is being designed for a 50-kHz bandwidth.

To control the field level in the accelerator, a monitor loop in the tank samples the rf field. This rf signal (tank amplitude feedback) is detected to produce a dc level proportional to the tank field amplitude. This dc level is compared with an FCS generated tank amplitude set point that corresponds to the desired field amplitude (Fig. 1). The difference between the tank amplitude set point and the feedback signal is the error. This error signal is sent to the PID amplitude controller of each PA driving that tank. The controller will change the attenuator setting of each amplifier chain such that the error signal goes to zero. At this time, each PA will be providing the required amount of power to the linac. This amplitude control loop will have a 10-kHz bandwidth.

High-Power Amplifier

Amplification from 100 W to 600 kW will be accomplished by several stages of vacuum tube amplifiers. A preliminary design study[5] has been done to determine the configuration for the high-power system.

The tube line-up is shown in Fig. 6. The final amplifier will be the EIMAC 8973 (formerly X2170) power tetrode. Preliminary design has been done for a 600-kW cw system at 80 MHz. The system will have a 3-dB bandwidth of 200 kHz. Linearity should be better than 0.37%.

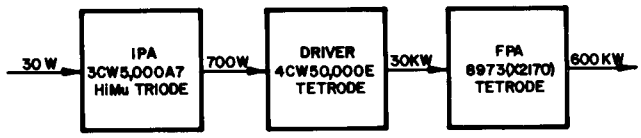

Fig. 6. Power amplifier tube line-up.

Prototype

A prototype FMIT accelerator capable of producing 5-MeV H_2^+ particles is under development now at LASL. This accelerator will require four rf amplifier chains to supply the necessary energy for beam acceleration.

The rf system for the FMIT accelerator at Hanford must be designed for 85% availability. To achieve this, each accelerator tank will use one more than the minimum number of power amplifiers necessary to drive it. This means that if one amplifier chain fails, the output of the remaining amplifiers can be increased to compensate for the loss without having to shut down the accelerator.

Acknowledgement

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