A NEW DESIGN OF PROFILE GRID ELECTRONICS WITH HIGH PERFORMANCE

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At the Unilac beam profiles are measured at about 100 locations by means of profile grids. In order to eliminate the elaborate service for off-set adjustments a new circuit for the processing of pulsed current signals has been designed. Current sensitivity was also improved. The time between current pulses is utilized for automatic drift compensation. For the anticipated time-shared operation of the Unilac and for simultaneous display of several beam profiles, a fast solid state multiplexer has been developed, which is capabale of switching currents down to 100 pA with good linearity. The paper describes the newly designed amplifier circuits including the automatic off-set compensation and the FET-current multiplexer. The complete electronics is controlled by a microprocessor which is integrated into the system. A description of the microprocessor board and the software is given as well.

Introduction

At linear accelerators like the Unilac the requirements on a versatile beam profile measurement system are rather high and can be summarized as follows:

- wide range of currents must be processed because of the large spectrum of ions which have to be accelerated,
- high sensitivity in the lowest current range in order to detect very small currents of highly charged ions or even ions of rare isotopes extracted from the ion source by using natural isotope mixtures as sputtering materials or burning gas, respectively,
- rather short signal integration times on the order of 0.5 - 10 ms as given by the duty cycle of the machine,
- fast signal processing in order to monitor the profiles of various ions with respect to the anticipated time share operation of the Unilac,
- fast range setting caused by pulse to pulse variation in intensity in the time share mode,
- fast switching of the complete analog signal processing electronics to various grids in order to observe multiple profiles along the machine at nearly the same time as needed for example in beam alignment procedures,
- modular design with respect to the number of channels (= number of wires in a grid) which have to be implemented,
- universal interfaces to the control system including local intelligence in order to control the electronics by simple commands,
- automatic off-set adjustment to avoid time consuming maintenance and service.

The new grid electronics developed at GSI fulfills the requirements and will be described in the following.

General description

A block diagram of the electronics is shown in Fig. 1. Up to 4 harps with a maximum of 2x48 wires each are connected to a newly developed fast FET-multiplexer. The signals of the selected harp are fed to high quality current to voltage converters followed by integrators. The integrated output signals are scanned by an analog multiplexer and digitized by the ADC.

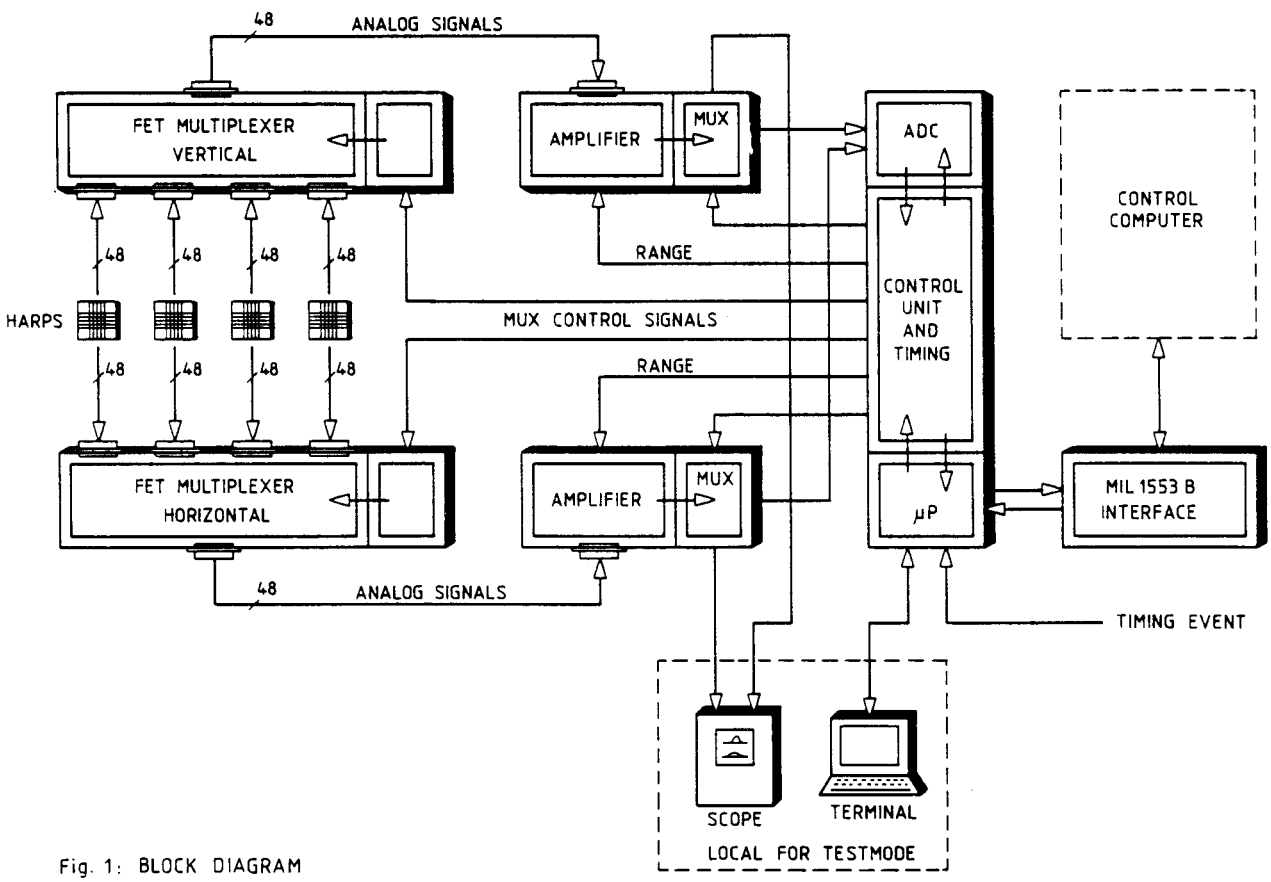


Fig. 1: BLOCK DIAGRAM

A microprocessor controls the range selection, the timing and the multiplexers. Digitized data including the appropriate range information are stored in a RAM integrated into the microprocessor system. The interface to the main control system is also controlled by the microprocessor via the local VME-system and a serial Mil 1553 B link. The whole system may be synchronized by timing pulses or event coding. For analog signal observation and trouble shooting an oscilloscope together with a remote terminal for the implementation of test- and command procedures may be used.

FET-Multiplexer

To prepare for the time shared operation of the Unilac (pulse to pulse ion or energy switching, compare Ref. 1) and the arising need for simultaneous display of several beam profiles, a fast solid state multiplexer has been developed which is capable of switching currents down to 100 pA with good linearity. The FET multiplexer uses new-on-the-market elements of bilateral FET-switches which are controlled by infrared light from an on-chip LED. The optical isolation of the FET-switch from the LED ensures low current losses in the pA-range. Two switches are driven in a complementary mode in order to always provide a low impedance path to ground - otherwise the incident ion beam current will build up exceedingly high voltages. The impedance ratio of the two paths is > 10E6 so that current losses during measurements or current leakages to the output at off-times are negligible.

For use with profile grids a reconfigurable multiplexer unit of 4 x 48 inputs has been developed. It can handle input currents of 100 pA to 100 µA at current errors of about 10 pA. Switching times are less than 50 µs.

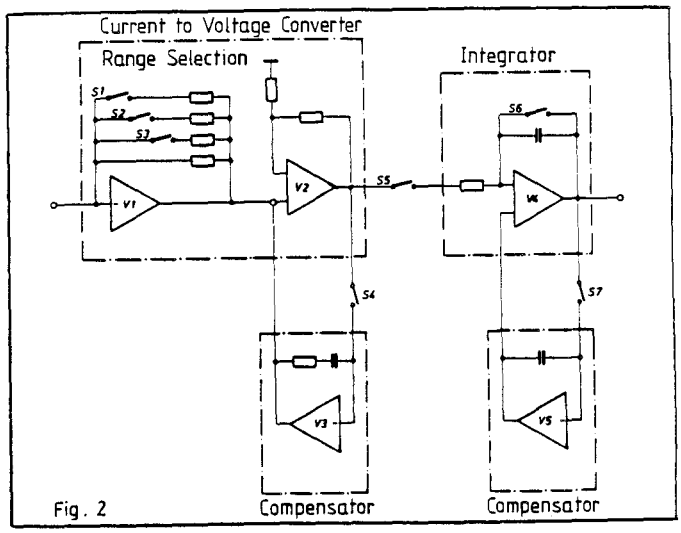
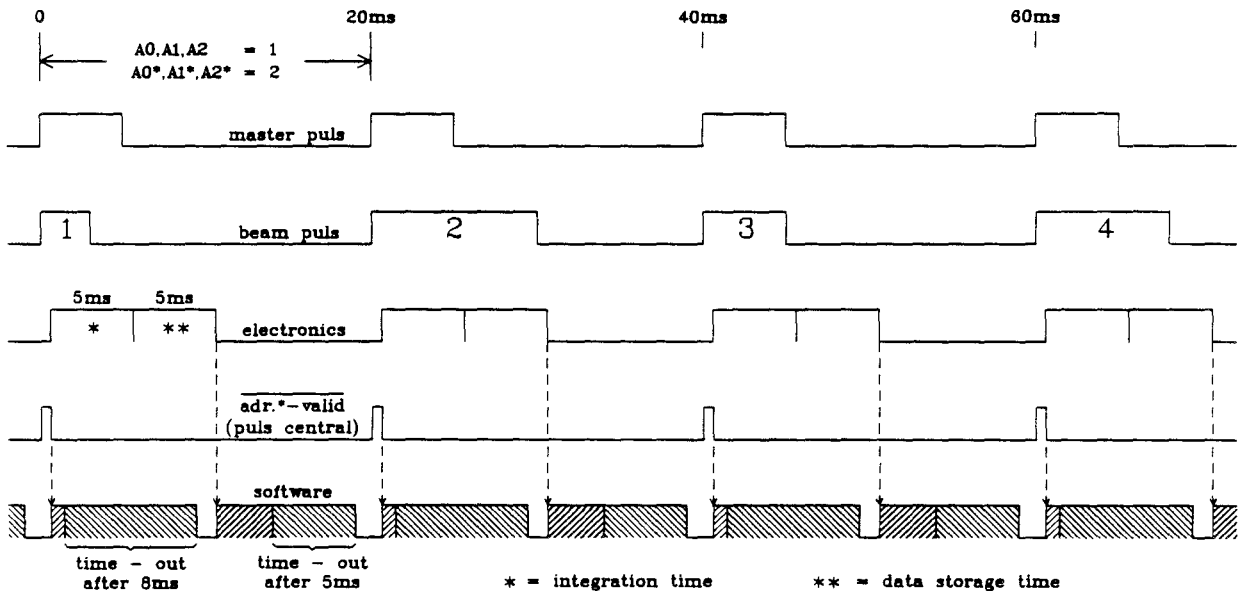


Fig. 2

Analog Signal Processing

Figure 2 shows the main parts of the analog signal processing unit. 12 ranges in steps of 1:2:5 may be selected for the current to voltage converters (V1) by hexadecimal coded commands. Including the constant gain of the following stages and considering an integration time of 5 ms conversion ratios from 20 nA/10 V up to 100 µA/10 V can be obtained. The time between pulses lends itself to be utilized for automatic drift compensation. Two operational amplifiers (V3, V5) in conjunction with two capacitors are provided to act as compensate-and-hold stages by forcing the outputs of the circuits to zero between beam pulses and maintaining the corrective voltages constant during the pulses. This operation is controlled by the switches S4 and S7.



gain and grid - address (number) to the electronics

wait for command from the control - electronics (SE)

data readout and data processing (96 wires, automatic gain)

transmit of data to the control - electronics (SE)

PROFIL GRID PROGRAM

USED BY THE BEAM DIAGNOSTIC MICROCOMPUTER (INTEL 8085)

TIMING DIAGRAM (Fig.3)

The signal processing system for one wire consists of seven chips and is packed onto a small board, eight of which fit to a motherboard in a plug-in housing.

Microprocessor control

A small cash-box with a microcomputer system has been developed at GSI and integrated into the profile grid electronics. The standard version of the system consists of:

- Processor INTEL 8085 A (clock = 3.072 MHz),
- 3 timers,
- 10 free selectable hardware-interrupts,
- 3 V24-interfaces (Rs 232),
- 6 x 8 Bit I/O-ports (2 x INTEL 8255),
- 16 Bit IN and 16 Bit OUT in handshakemode,
- 48 kByte free usable RAM or ROM memory,
- Monitor-program (GSI-Monitor V2.3).

Up to 4 profile grids selected via the FET-multiplexer measuring the profiles of up to 4 different beam pulses are handled by the microcomputer system. The timing digram of Fig. 3 shows the hard-and software activities during the 20 ms cycle of the accelerator. In order to synchronize the measurement cycle exactly to the acceleration process the interrupt vector with the highest priority (IR2) has been connected to the main pulser.

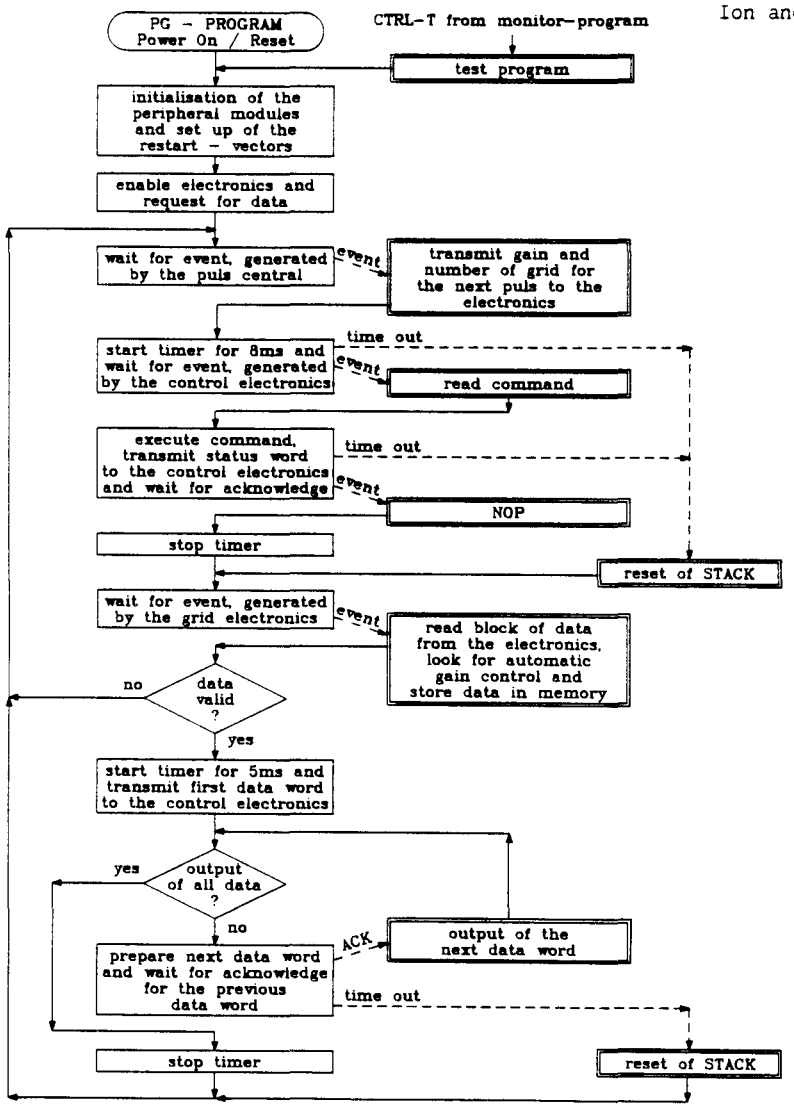


Fig. 4: Software Flow-Diagram

The software modules for the control of the electronics and the triggering of the measurement cycle as well as the software for the communication with the interface are initialized dynamically via vectored interrupts (IR3-IR12). The software activities during one cycle are shown very schematically in the flow diagram of Fig. 4.

After an IR2-interrupt has been received a read-out of the code representing the actual kind of beam pulse (A_0 - A_2) is performed. The same procedure holds concerning the information about the next beam pulse (coded in A_0* - A_2*). Then the microprocessor transmits the gain and grid number for the next pulse to the electronics and starts the actual measurement cycle of 8 ms. At the same time the transmission line to the control system via the so-called SE-interface which is integrated in the local VME-system is enabled to allow exchange of command procedures during the 8 ms cycle. At the end of the measurement cycle the transmission line is disabled. The microprocessor then reads the measured profiles from the electronics and stores the data including the relevant information about the cycle in the RAM. After this operation the transmission line is enabled again and the complete data are transferred to the host computer in a block transfer mode. The system then is ready for the next beam pulse.

References

[1]Glatz, J., The Unilac as a Fast Switching Variable Ion and Energy Accelerator, these proceedings.